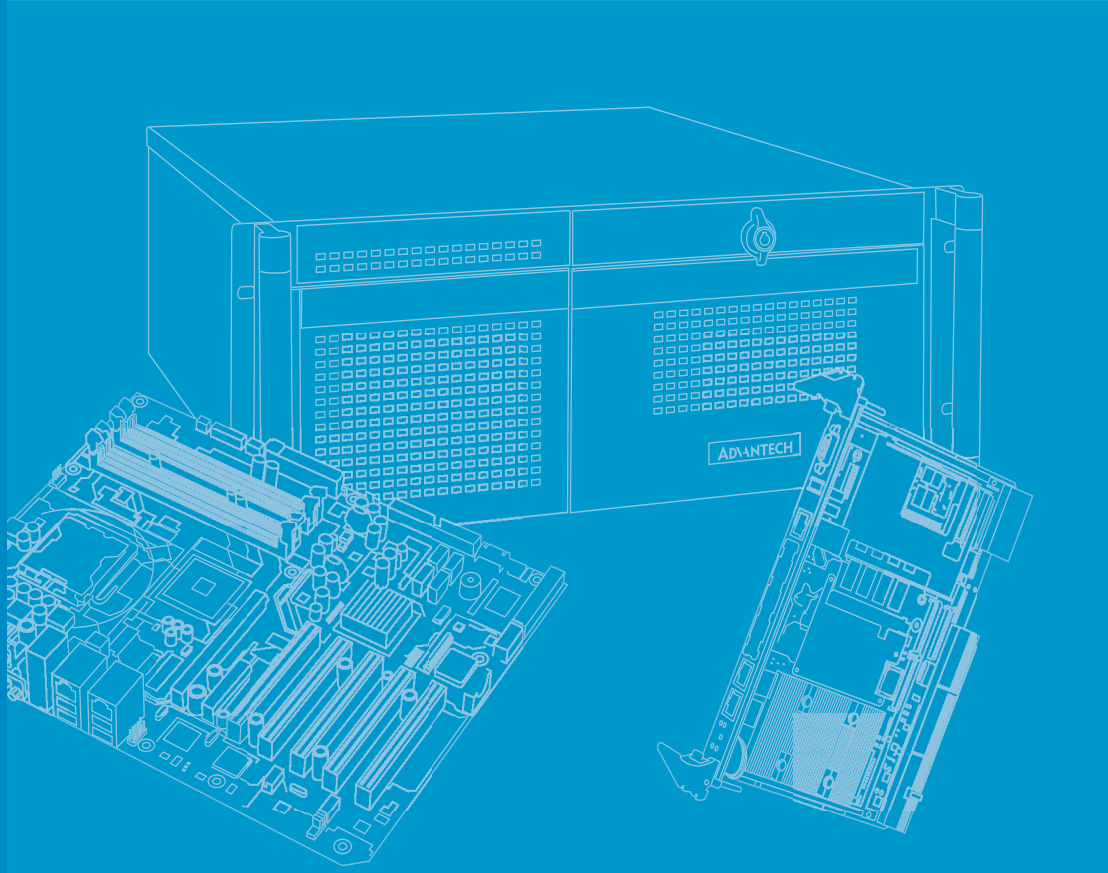

User Manual

MIC-6330

3U OpenVPX CPU Blade with Intel® Xeon® Processor E3v5 and E3v6 family

ADVANTECH

Enabling an Intelligent Planet

Copyright

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Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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Printed in Taiwan May 2018

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

- MIC-6330 all-in-one single board computer (heatsink included) x1
- Daughter board for front panel x1 (Assembled, only available on the specific SKU)
- Warranty certificate document x1
- Safety Warnings: CE, FCC class A

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -40° C (-40° F) OR ABOVE 85° C (185° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don’t touch any components on the CPU card or other cards while the PC is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could benefit from improvements or corrections. We appreciate your valuable input in helping make our products better.

Contents

Chapter 1

Hardware Configuration

This chapter describes how to configure the MIC-6330 hardware.

1.1 Introduction

Based on the Intel® Xeon® E3 Lv5 and Lv6 embedded platform, the MIC-6330 builds on the success of Advantech's 6U VPX boards, and is the first 3U VPX product launched by Advantech. Together with the Intel® processor, the MIC-6330 offers intense computational ability in a very compact form factor. The MIC-6330 provides configurable connectivity (up to four ports) of PCI Express via the backplane to the highest performance mainstream peripherals and I/O cards, and vast I/O functions for extended inter connectivity and controllability.

The MIC-6330 meets various computing needs, including vPro™ and workstation capabilities, by using the Intel® CM236/CM238 PCH. The MIC-6330 offers high storage capacity at up to SATA 6Gbps transfer speed. Four USB2.0 ports and one USB 3.0 port to the backplane fulfill requirements for extra I/O ports or storage, up to 5Gbps data rate. Four GbE ports (two ports configurable as SERDES) support system level IP connectivity, and the UART interfaces (RS-232/422/485 selectable) can be leveraged as an interface to legacy devices and consoles. Like Advantech's 6U VPX products, the MIC-6330 supports multiple displays, and the maximum resolution of the MIC-6330 is 4K, empowered by the Intel® integrated graphics engine. The MIC-6330 also offers a High Definition Audio to the backplane interface for media demands.

With the standard ruggedized convection cooled heatsink or the optional air-cooled heatsink, the MIC-6330 is tailored for harsh environmental applications and adaptable to various chassis designs. The industrial NAND Flash, and the soldered onboard DDR4 ECC memory chips are appropriate for a variety of vehicle applications for the maximum reliability.

The MIC-6330 is sophisticated and suitable for various purposes. An onboard X8D XMC site with PCIE x8 gen.3 connectivity can host high speed offload or I/O mezzanines for project-specific applications. For applications that need the maximum expandability, the XMC interface can be modified to add another DisplayPort and the 2 more UART. The optional front I/O module facilitates the development and qualification process, and also enables the possibility of front panel access.

1.2 MIC-6330 SKU Introduction*

Table 1.1: Processor Type

MIC-6330 Model Number	CPU	# cores	Cooling.	Onboard DIMM capacity	Onboard Flash NAND flash capacity	Front Panel I/O	XMC
MIC-6330-A1A4E	E3-1505Lv5	4	Convection cooling	16GB	64GB	Yes	No
MIC-6330-A1C4E	E3-1505Lv5	4	Conduction cooling	16GB	64GB	No	No
MIC-6330-A2C4E	E3-1505Lv5	4	Conduction cooling	16GB	64GB	No	Yes
MIC-6330-B1C4E	E3-1505Lv6	4	Conduction cooling	16GB	64GB	No	No

*: Please contact the local Advantech representatives for the different combinations of CPU's and heatsinks.

1.3 Specifications

1.3.1 OpenVPX Interface

The MIC-6330 is compliant with the OpenVPX MOD3-PAY-2F2U-16.2.3-3 profile. A PCIE port with 8 lanes is provided in the P1 Data plane. Two lanes of 1GBase-T (can be configured to SerDes, on request) are used for the control plane.

1.3.2 CPU

The MIC-6330 supports the Intel® Xeon® E3 v5 and E3 v6 family 1505 series processor family with clock frequencies up to 3.0 GHz. Intel Xeon® E3 v5 & v6 family processors integrate the embedded graphic controller Intel® HD Graphics P530 (E3v5) or P630 (E3v6). With graphic controller, the MIC-6330 supports OpenGL 4.4, DirectX 12 and also OpenCL 2.0 to enhance 3D graphic processing. The CPU provides more performance when Intel® Turbo Boost Technology 2.0 is required. Turbo Boost automatically activates when the OS requests the highest processor performance state. With Intel HT Technology, the MIC-6330 can run demanding applications simultaneously, while maintaining system responsiveness.

1.3.3 Processor

The Xeon E3-1505Lv5 and E3-1505Lv6 are the default CPU for the MIC-6330. Please contact your distributor or local Advantech branch for the availability of the other E3/ i7 SKU.

Table 1.2: Processor Type

Intel CPU Model Number	CPU architecture	# cores	Graphic Engine	Freq.	Cache	DMI	CPU TDP
E3-1505Lv5	Skylake (14nm)	4	Intel® HD Graphics P530	2.8GHz (max)	8MB	8 GT/s	25W
E3-1505Lv6	Kabylake (14nm)	4	Intel® HD Graphics P630	3.0GHz (max)	8MB	8 GT/s	25W

Note! *Because power consumption and thermal restrictions vary between different VPX systems, please double check these items before installing a higher speed CPU not specified in the table above.*

1.3.4 BIOS

An 16 Mbyte SPI flash contains a board-specific BIOS (from AMI) designed to meet industrial and embedded system requirements. MIC-6330 has a redundant BIOS as the backup, and the two BIOS's can be switch via IPMI command. Please refer to the chapter 3.9 BIOS redundancy for the details.

1.3.5 Chipset

The Intel Mobile CM236 (E3v5)/ CM238 (E3v6) chipset integrates several capabilities to provide flexibility for connecting I/O devices. The Intel CM236 (E3v5)/ CM238 (E3v6) chipset offers fast access to peripheral devices. It delivers outstanding system performance through high bandwidth interfaces such as PCI Express Gen3, Serial ATA and Integrated USB 3.0. Intel® Rapid Storage Technology provides excellent performance and expandability for MIC-6330.

1.3.6 Memory

The MIC-6330 has 16 GB of onboard with ECC support DDR4 memory. Please contact your distributor or local Advantech branch for the availability of the different memory capacity.

1.3.7 Ethernet

The MIC-6330 uses the Intel I350 Ethernet controllers connecting to P1 to provide two ports of 1000Base-BX Ethernet connectivity to the control plane, and two ports of 10/100/1000Base-T to the backplane. The MIC-6330-A1A4E has a

10/100/1000Base-T Ethernet port on the front panel from the Intel® I210 Ethernet controller.

- Front I/O: 10/100/1000Base-T (RJ-45)
- Control plane: 1000Base-BX
- User define pins(P1): 10/100/1000Base-T

1.3.8 Storage Interface

The MIC-6330 supports three ports of SATA III interfaces. A SATA III interface is routed to the onboard soldered, industrial NAND FLASH (Only gen. 1 device is available now). The rest of two SATAIII are routed to P2. The default onboard flash capacity is 64GB. For different onboard flash capacity, please contact your local Advantech branch or distributor to offer the customized option.

1.3.9 Serial ports

Four UART ports are routed to the backplane via the P2 connector. Two of the four UART ports are from the BMC, and can be configured as RS232 or RS422. However, the 2nd UART is occupied by BMC serial over LAN function. If you need the 2nd UART of the BMC, and the SOL function isn't needed, please contact your Advantech representative for the 2nd UART availability. The rest two are from the FPGA, with Tx,Rx, RTS & CTS only, and need extra transceiver while implementing in the RIO. These UART ports from the FPGA are co-layout with the XMC pins, and are not available while the XMC SKU is used.

1.3.10 USB Ports

Two USB 3.0 compliant ports with fuse protection are provided. One USB2.0/3.0 port is available on the front panel of MIC-6330-A1A4E. All of the MIC-6330 has two USB 2.0 ports and a USB3.0 routed to the rear I/O module via the P1 connector. Two USB2.0 ports are available on the P2 connector.

1.3.11 LEDs

Four LEDs are provided on the front panel as follows:

- One blue LED indicates hot swap. The blue color indicates that the board may be safely removed from the system.
- One yellow LED indicates HDD status, The blinking LED indicates HDD activity.
- One LED provides power status. When the LED is green, it means power is provided to the board.
- Last one provide the BMC status. The LED is green while the BMC is present.

1.3.12 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control.

The programmable time interval is from 1 to 255 seconds. This function is enabled by default in the SKU with IPMI management. If you need this function in the SKU without IPMI management, please contact your local FAE or salesperson.

1.3.13 Optional Rear I/O Modules

Please contact your local Advantech branch or distributor for inquiries about a customized RIO option.

1.3.14 Mechanical and Environmental Specifications

- **Operating temperature:** -40 ~ 70°C (32 ~ 131°F)

Note! *The operating temperature range of the MIC-6330 depends on the installed processor and the airflow through the chassis.*

- **Storage Temperature:** -55 ~ 105°C (-67 ~ 221°F)
- **Humidity:** 95% @ 40°C (non-condensing)
- **Humidity (Non-operating):** 95% @ 85°C (non-condensing)
- **Vibration:** VITA47, V2
- **Shock:** 40G (with the onboard flash only)
- **Altitude:** up to 50,000m above sea level
- **Board size:** 233.35 x 160 mm (6U size), 1-slot (4 TE) wide
- **Weight:** 0.95 kg

1.3.15 Compact Mechanical Design

The mechanical design of MIC-6330 is compliant with VITA 48.2, REDI specification. The MIC-6330-A1C4E is Advantech's standard ruggedized convection cooled SKU. Please check with your distributor or local Advantech branch for the feasibility of a customized conduction cooled heatsink design.

1.3.16 PCIE Bridge

The MIC-6330 uses a PLX PEX8725 component, a 24-lane, 10-port, PCIE Gen 3 switch device as a gateway to an intelligent subsystem. When configured as a system controller, the bridge acts as a standard transparent PCI Express Bridge. The MIC-6330 receives power from the backplane, and supports a rear I/O. The PLX PEX 8725 offers the following features:

- PCI Interface
  - Full compliance with the PCI Local Bus Specification, Revision 3.0
  - PCI Power Management Spec, r1.2
  - PCIE reference clock to the backplane
- Supports transparent and non-transparent mode of operations. Please contact your local Advantech representative for the different firmware content
- Supports forward and reverse bridging
- 64-bit, 66MHz asynchronous operation
- End-to-end CRC (ECRC) protection
- Failover support, can be configured for 1+1 redundancy or N+1 redundancy.

Please consult the PLX PEX 8725 data book for details.

1.3.17 I/O Connectivity

On the MIC-6330-A1A4E, the front panel I/O provides a RJ-45 Gigabit Ethernet ports, a USB 3.0 port, and a VGA connector.

Part Number	I/O ports		
MIC-6330-A1A4E	Display	USB	Ethernet (RJ45)
	VGAx1	3.0x1	1

Rear I/O connectivity is available via the following VPX connectors:

- **P1:** A PCIE port with 8 lanes, can be configured to 4 x 2 or 2 x 4*. Two USB2.0 or a USB3.0. Two 10/100/1000Base-T ports and two 1000Base-BX ports.
- **P2:** Two SATA III ports, A HDA audio, ports, two USB2.0 ports, one DisplayPort and two UART (RS232/RS422) are provided**. Eight differential pairs for XMC are provided on the SKU with XMC. For the SKU without the XMC X8D pin out, the 3rd, 4th UART and the 2nd Displayport are also available on the P2 connector.

  *Please contact the local Advantech representative for configurability
  **Please refer to 1.3.9

1.3.18 XMC (Switched Mezzanine Card) VITA 42 Compliant

The MIC-6330 supports one XMC site that is fully compliant with the VITA 46.9 PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard specification of X8D pairs.

1.3.19 RTC and Battery

The RTC module keeps the date and time. On the MIC-6330 model the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3V, 210mAH).

1.3.20 Trusted Platform Module

MIC-6330 uses the 9665XT2 from Infineon for the Trusted Platform Module solution. The TPM implementation has achieved CC EAL4+ certification, and is compliant to TPM Main Specification, Family "2.0", Level 00, Revision 01.16. Connecting to the LPC interface of the TPM, MIC-6330 has the advanced hardware security technology. The TPM supports the following features:

- True Random Number Generator (TRNG)
- Full personalization with Endorsement Key (EK) and EK certificate
- 24 PCRs (SHA-1 or SHA-256)
- 7206 Byte free NV memory
- Up to 3 loaded sessions (TPM_PT_HR_LOADED_MIN)
- Up to 64 active sessions (TPM_PT_ACTIVE_SESSIONS_MAX)
- Up to 3 loaded transient Objects (TPM_PT_HR_TRANSIENT_MIN)
- Up to 7 loaded persistent Objects (TPM_PT_HR_PERSISTENT_MIN)
- Up to 8 NV counters
- Up to 1 kByte for command parameters and response parameters
- Up to 768 Byte for NV read or NV write
- 1280 Byte I/O buffer
- Built-in support by Linux Kernel Version 3.10 and higher

1.3.21 IPMI

The MIC-6330 uses Intelligent Platform Management Interface (IPMI) to monitor the health of the entire system. An Aspeed AST1010 microcontroller provides BMC functionality to interface between the system management software and platform hardware. Full IPMI details are covered in Chapter 3.

1.3.22 Key Features

- Advantech Integrity Sensor
- Based on Advantech IPMI Core, designed for xTCA, CPCI and VPX
- IPMI 1.5 and IPMI 2.0 Specification compliant
- IPMI-over-LAN
- Serial-over-LAN
- KCS interface for direct IPMI communication between Operating System and BMC
- BIOS fail over, including BIOS watchdog
- Full BMC Watchdog support as defined in the IPMI specification
- Full BMC Firmware redundancy
  - Manual roll back
  - Automatic roll back if update failed
- HPM.1 for in field updates, supporting:
  - BMC Bootloader
  - BMC Firmware
- UART muxing between all serial interfaces for easy console access (UART1, UART2 only)
- Additional sensors for hardware monitoring

1.4 Functional Block Diagram

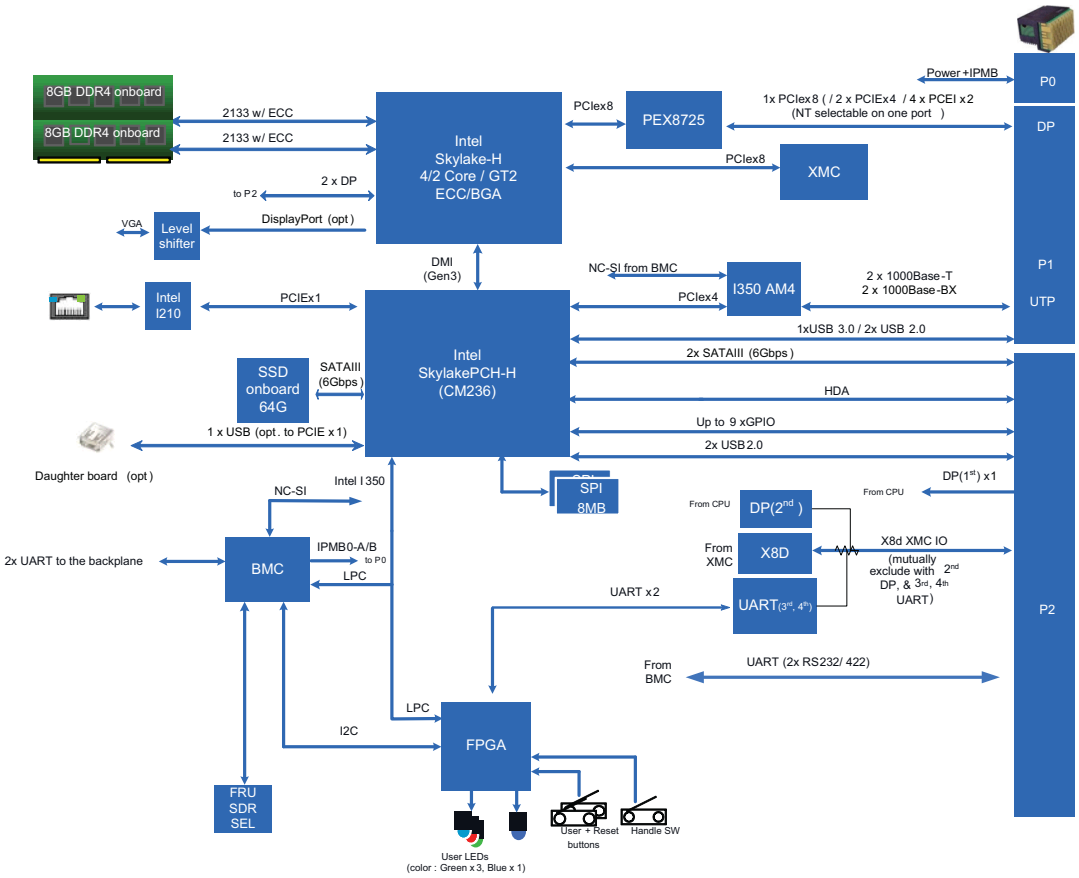


Figure 1.1 MIC-6330 functional block diagram

1.5 Board Map

The Main components, jumpers, switches and thermal sensors location are shown in the figure below.

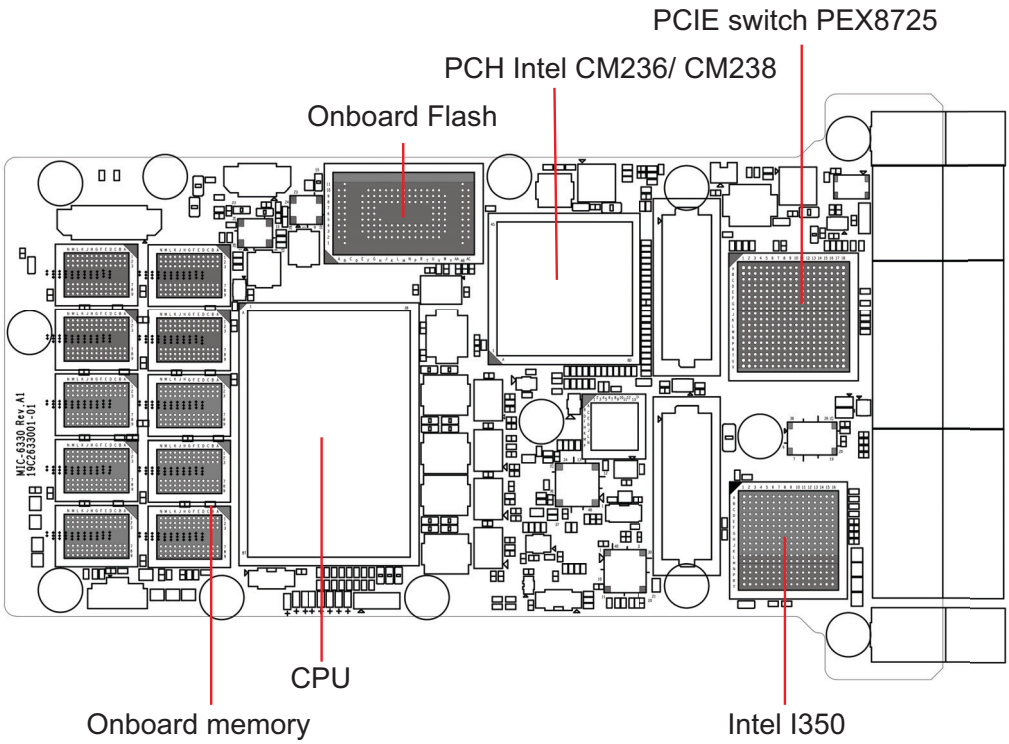


Figure 1.2 Board map

1.6 Connector Definitions

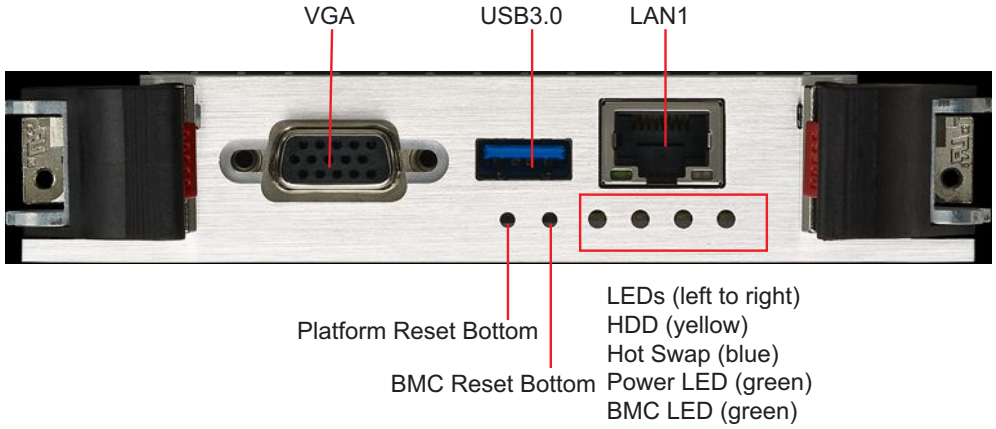


Figure 1.3 MIC-6330 Front Panel Ports, Indicators and Buttons

The MIC-6330 supports three BMC controlled front panel LEDs.

Table 1.3: Front Panel LEDs

LED	Color	Description
1	Blue	Hot swap indicator
2	Green	BMC indicator
3	Green	Power indicator

The LED's act as the following behaviors.

Item	Meaning	Color	Behavior
Power	Power on	Green	LED On
HDD	HDD active	Yellow	Blinking
Hot swap	Ready to perform hot swap	Blue	LED On
BMC act LED	BMC active	Green	LED On

1.6.1 USB Connectors

The MIC-6330 provides both Universal Serial Bus (USB) 3.0 & 2.0 channels. A USB 3.0 is on the front panel. Two USB 2.0 channels are routed to the P2 connector, and the two USB2.0 and one USB3 to the P1 connector (alternative). The USB interface provides complete plug and play, and hot attach/detach for up to 127 external devices. The MIC-6330 USB interface complies with USB specification R3.0 and is fuse protected (5V @ 1.1A). The USB interface can be disabled in the system BIOS setup. The USB controller default is set to "Enabled". Because the limited space available on the front panel, some USB stick with too wide width (greater than 17 mm) may have interference with the VGA cable, please select the USB stick with proper width.

1.6.2 Serial Ports

The BIOS Advanced Setup program covered in Chapter 2 provides a user interface for features such as enabling or disabling the ports, and setting the port address. Many serial devices implement the RS-232 standard in different ways. If you have problems with a serial device, be sure to check pin assignments for the connectors. The IRQ and address range for these ports are fixed. However, if you wish to disable the port or change these parameters later, you can do this in the system BIOS setup.

1.6.3 Ethernet Configuration

The MIC-6330 is equipped with a high performance, PCI-Express based, network interface controller, the I350, which provides two fully compliant IEEE802.3 10/100/1000Base-TX Ethernet interfaces and two 1000Base-BX to the backplane(P1). A GbE interface is available on the front panel by the I210.

1.6.4 System Reset and BMC Reset Button

The MIC-6330 provides a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry. It does not reset the system management (IPMI) related circuitry. A separate BMC reset button on the front panel is provided for the BMC and related hardware.

1.7 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your VPX chassis before you work on it. Don't touch any components on the CPU board or other boards while the VPX chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.8 Installation Steps

The MIC-6330 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins. Advantech recommends that you perform assembly at an anti-static workbench.

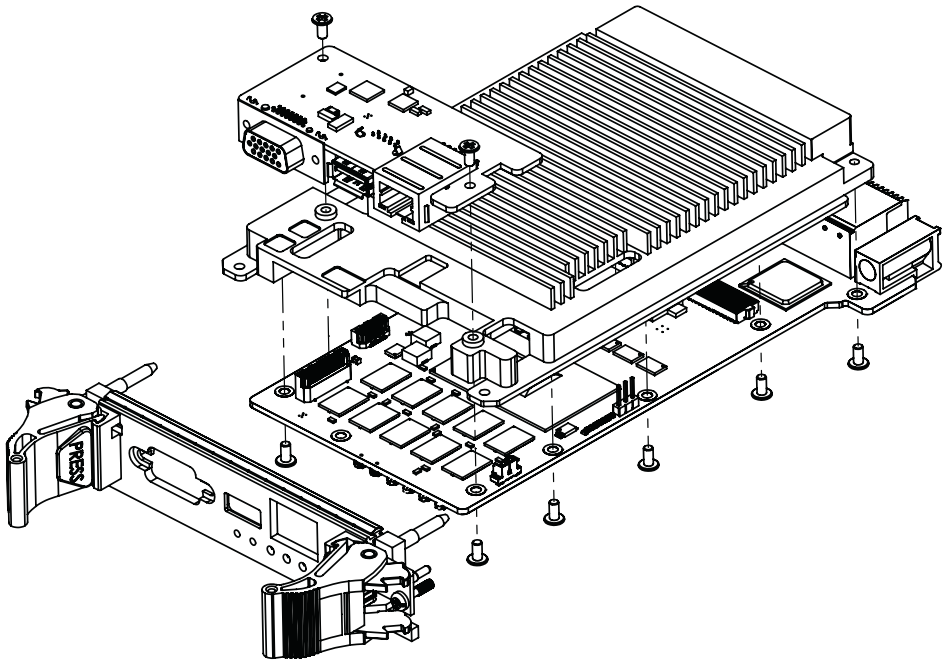


Figure 1.4 Complete assembly of MIC-6330 convection with the front I/O daughter board

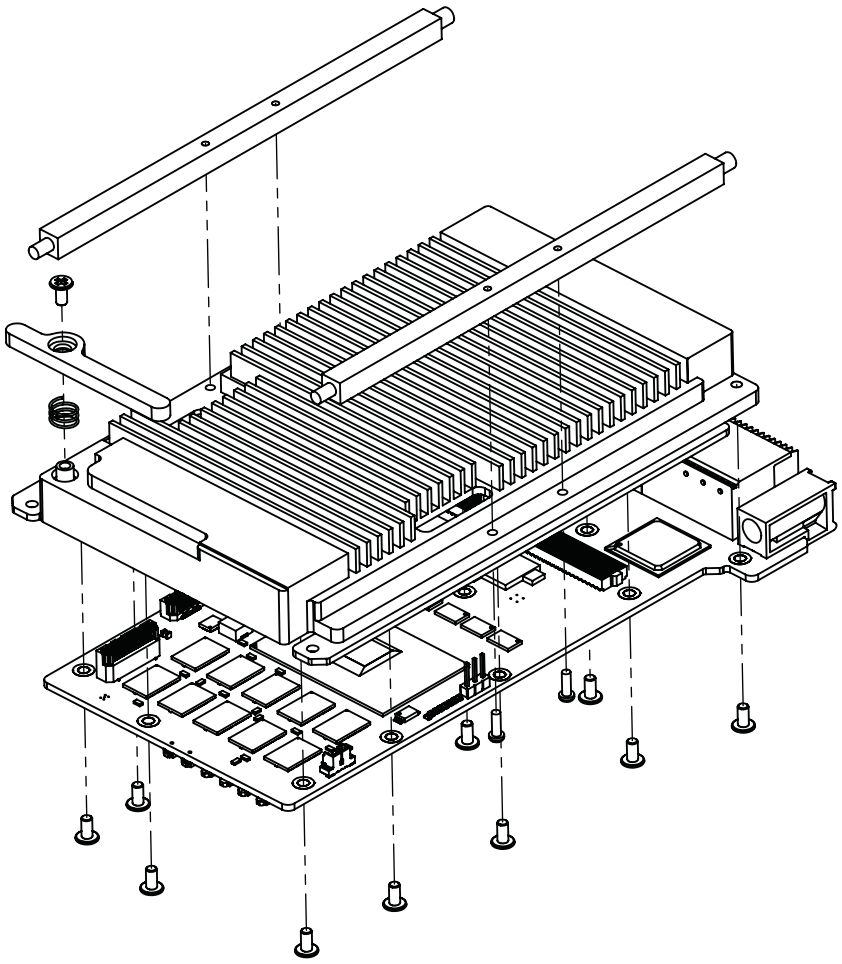


Figure 1.5 Complete assembly of MIC-6330

1.9 Battery Replacement

The Battery model number is CR2032M1S8-LF, a 3V, 210 mAh battery. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact your local Advantech sales office to check the availability.

1750129010 – BATTERY 3V/210 mAh with WIRE ASS'Y CR2032M1S8-LF

1.10 Software Support

Windows 10, Win 7 with XHCI driver populated and CentOS 7.2 Linux have been fully tested on the MIC-6330. Please contact your local sales representative for details for support of other operating systems.

Chapter 2

AMI APTIO BIOS Setup

This chapter describes how to configure the AMI APTIO BIOS (UEFI BIOS).

2.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for over a decade. In order to extend the features on the Intel® Grantley Platform, Advantech implements the latest AMI APTIO BIOS into the MIC-6330 to enhance its operating performance.

This section describes the UEFI compliant AMI APTIO BIOS, which has been specifically adapted to the MIC-6330. With the AMI APTIO BIOS Setup program, users can modify BIOS settings and control the special features of the MIC-6330. The setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the MIC-6330 setup screens.

The BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. Please see the following sections for instructions.

2.2 Entering Setup

Turn on the computer, and there should be a "patch" code displayed that shows the BIOS supporting the CPU. This will ensure that the CPU's system status is valid. After ensuring that users have a number assigned to the patch code, press <DEL> or <F2> and users will immediately be allowed to enter Setup.

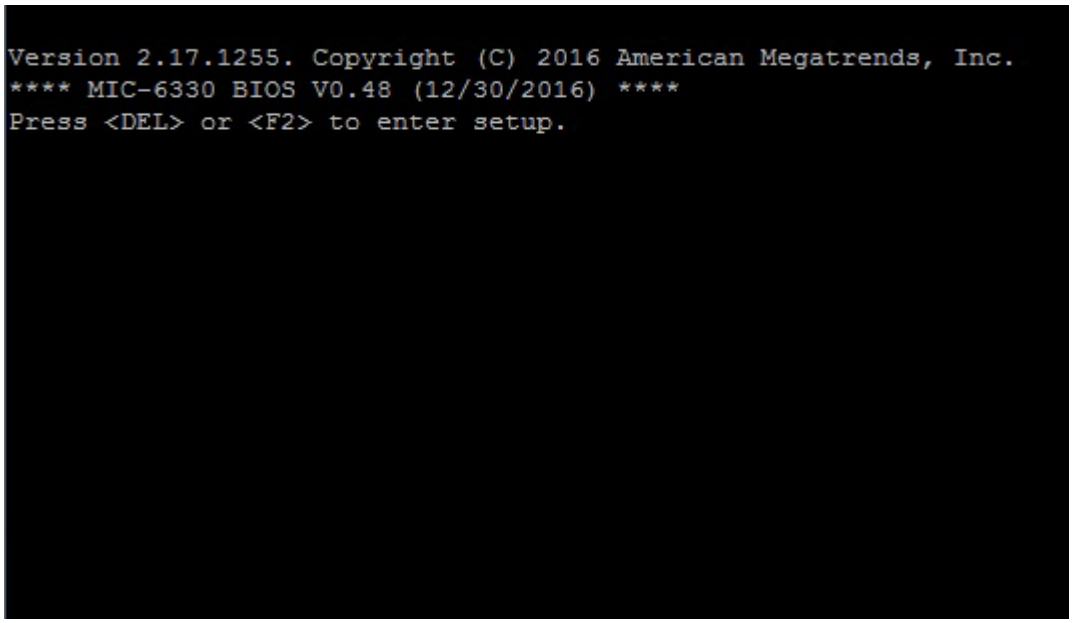


Figure 2.1 Press <DEL> or <F2> to run setup

2.2.1 Main Setup

When users first enter the BIOS Setup Utility, users will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured, the default setting is in bold. The right frame displays the key legend. Above the key legend is an area reserved for a text message.

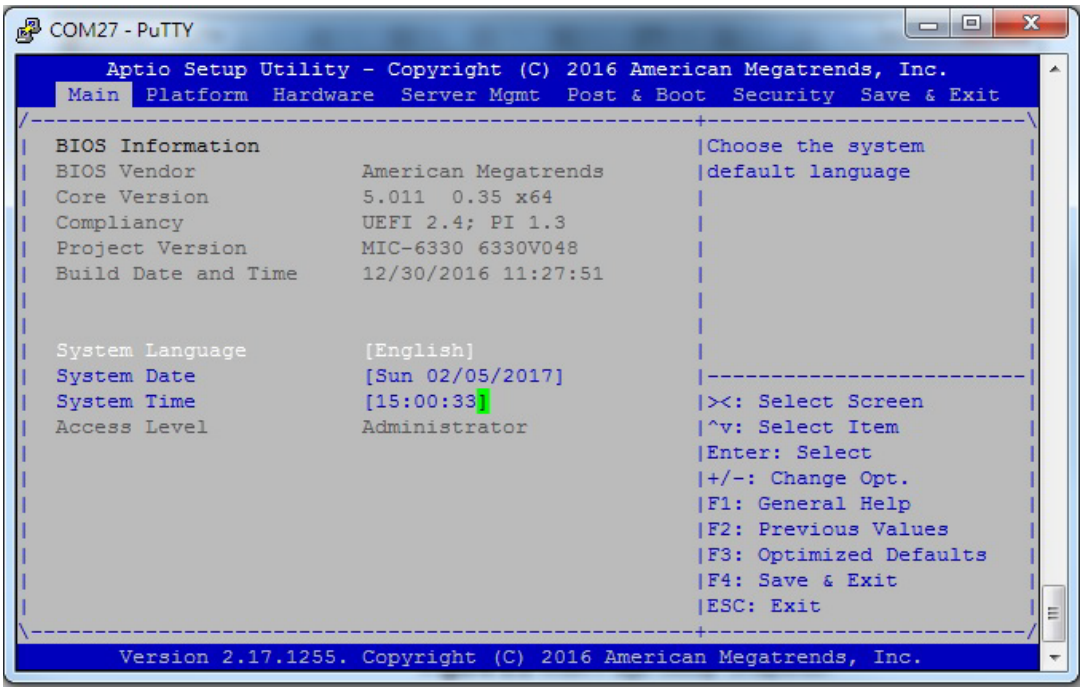


Figure 2.2 Main Page Setup Snapshot

Table 2.1: BIOS Menu: Main			
Feature	**Content**	**Description**	**Help text**
BIOS Vendor	American Megatrends	BIOS Vendor	N/A
Core Version	X.YYY	Display the BIOS Core version	N/A
Compliancy	UEFI X.Y; PI W.Z	Display the UEFI Platform Initialization version.	N/A
Project Version	MIC-6330 6330XYYY	Display BIOS version	N/A
Build Date and Time	mm/dd/yyyy hh:mm:ss	Display BIOS build date & time.	N/A
System Language	English	Choose the system default language.	Choose the system default language.
System Time	HH:MM:SS	Set the system time.	Use [+] or [-] to configure system time.
System Date	MM/DD/YYYY	Set the system date.	Use [+] or [-] to configure system date.
Access Level	Administrator User	Display currently access level	

- **System Date / System Time**

  Use this option to change the system date and time. Highlight System Date or System Time by using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.2.2 Platform Setup

Select the Platform tab from the MIC-6330 setup screen to enter the Platform setup screen. Users can select any of the items in the left frame of the screen, such as Serial Console, to go to the sub menu for that item. Users can display the Platform setup option by highlighting it using the <Arrow> keys. All Platform setup options are described in this section. The Platform setup screen is shown below. The sub menus are described on the following pages.

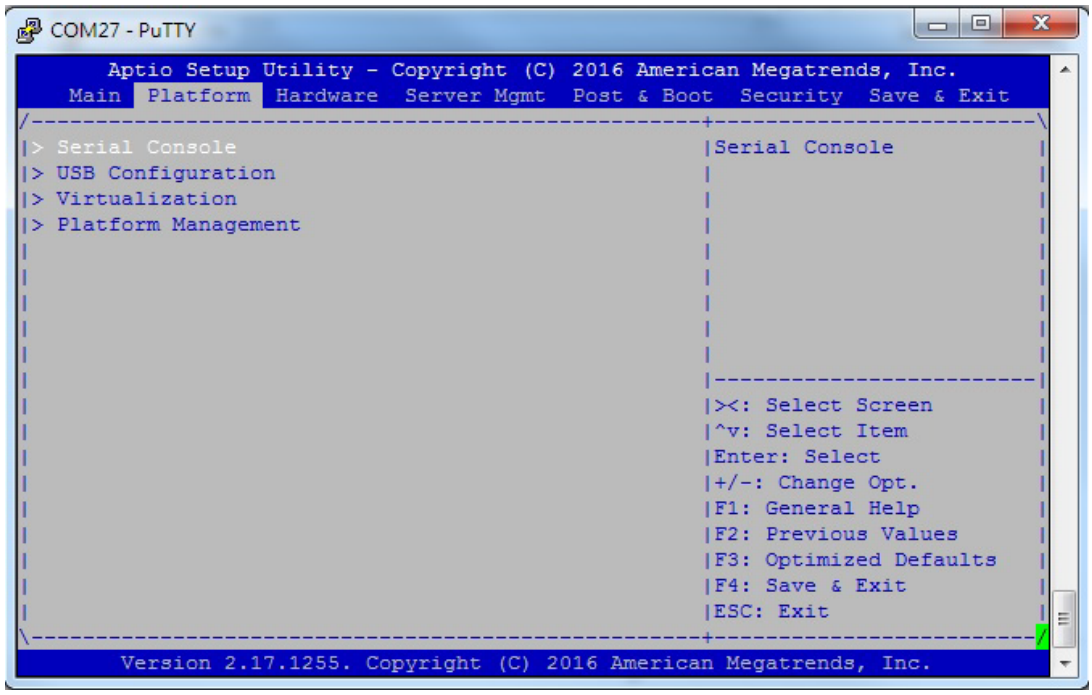


Figure 2.3 Platform Setup Snapshot

2.2.2.1 Serial Console

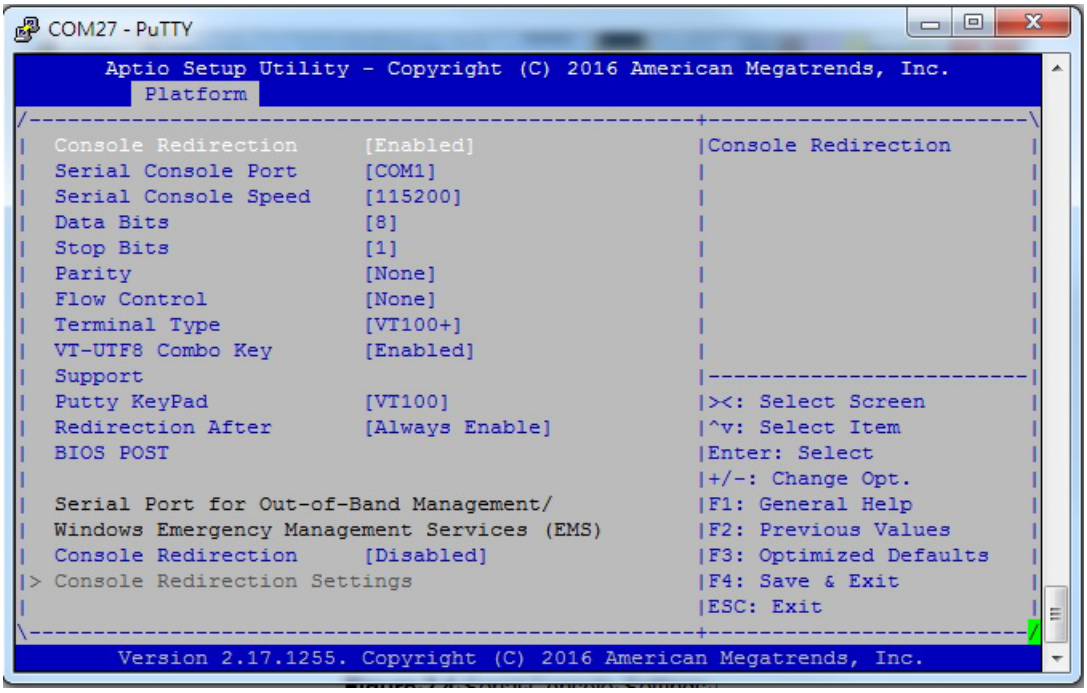


Figure 2.4 Serial Console Settings

Table 2.2: Serial Console Settings			
Feature	**Options**	**Description**	**Help text**
Console Redirection	Enabled Disabled	Enable or disable console redirection.	Console redirection.
Serial Console Port	COM1	Select serial port.	Select serial port.
Serial Console Speed	9600, 19200, 38400, 57600, **115200**	Configure serial port Baud rate for serial port.	Select serial port Baud rate.
Data Bits	7 8	Configure the number of data bits in each transmitted or received serial character for both serial ports.	Data Bits
Stop Bits	1 2	Configure the number of stop bits transmitted and received in each serial character for both serial ports.	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Parity	**None,** Even, Odd, Mark, Space	Configure if parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data for both serial ports.	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the number of 1's in the data bits is even. Odd: parity bit is 0 if the number of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Flow Control	**None,** Hardware RTS/CTS	Configure flow control for console redirection.	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Terminal Type	**VT100**, VT100+, VT-UTF8, ANSI	Configure the type of console emulation used.	Terminal Type for Redirection Via AMI Debugger. Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
VT-UTF8 Combo Key Support	**Enabled**, Disabled	Enable or disable VT-UTF8 Combo Key	Enable VT-UTF8 Combination Key Support for ANSI/ VT100 terminals
Putty KeyPad	VT100 LINUX XTERMR 6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	Always Enable Boot-Loader	The Settings specify if Boot-Loader is selected, then Legacy console redirection is disabled before booting to Legacy OS. Default value is always Enabled which means Legacy Console Redirection is enabled for Legacy OS.	The Settings specify if Boot-Loader is selected, then Legacy console redirection is disabled before booting to Legacy OS. Default value is always Enabled which means Legacy Console Redirection is enabled for Legacy OS.

2.2.2.2 USB Configuration

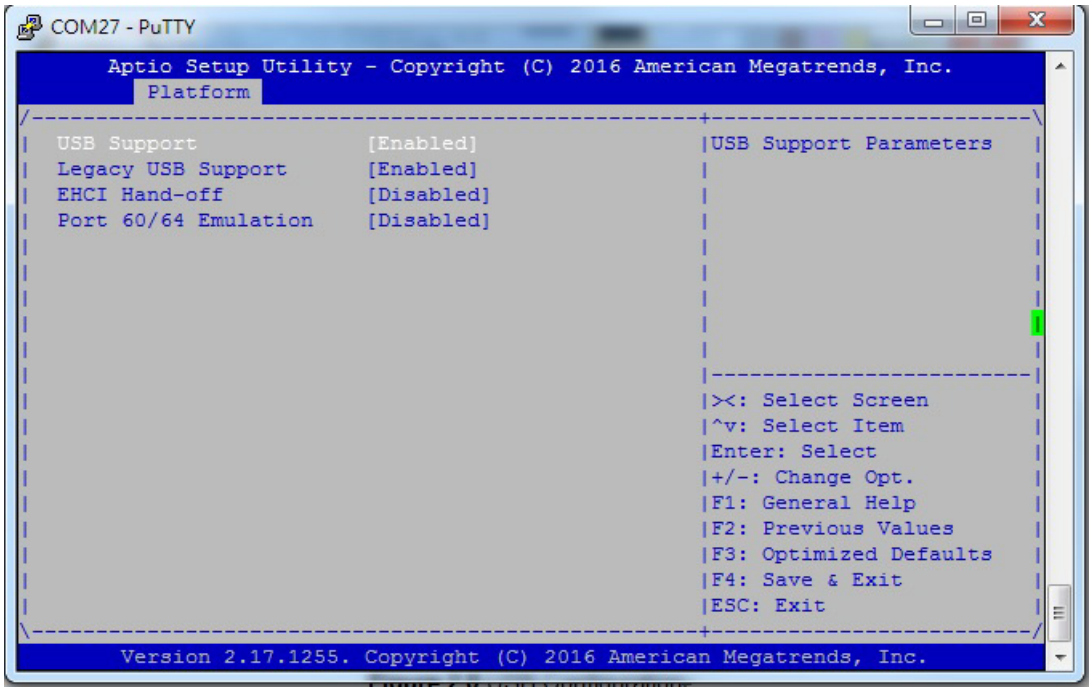


Figure 2.5 USB Configuration

Table 2.3: Serial Console Settings

Feature	Options	Description	Help text
USB Support	Disabled Enabled	Enable or disable USB function support	USB Support Parameters
Legacy USB Support	Enabled Disabled Auto	Enable or disable Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	Enable Legacy USB support. AUTO option disable legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
EHCI hand-off	Enabled Disabled	Enable or disable the EHCI hand-off for the Operations Systems without the ECHI hand-off support.	This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver
Port 60/64 Emulation	Enabled Disabled	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

2.2.2.3 Virtualization

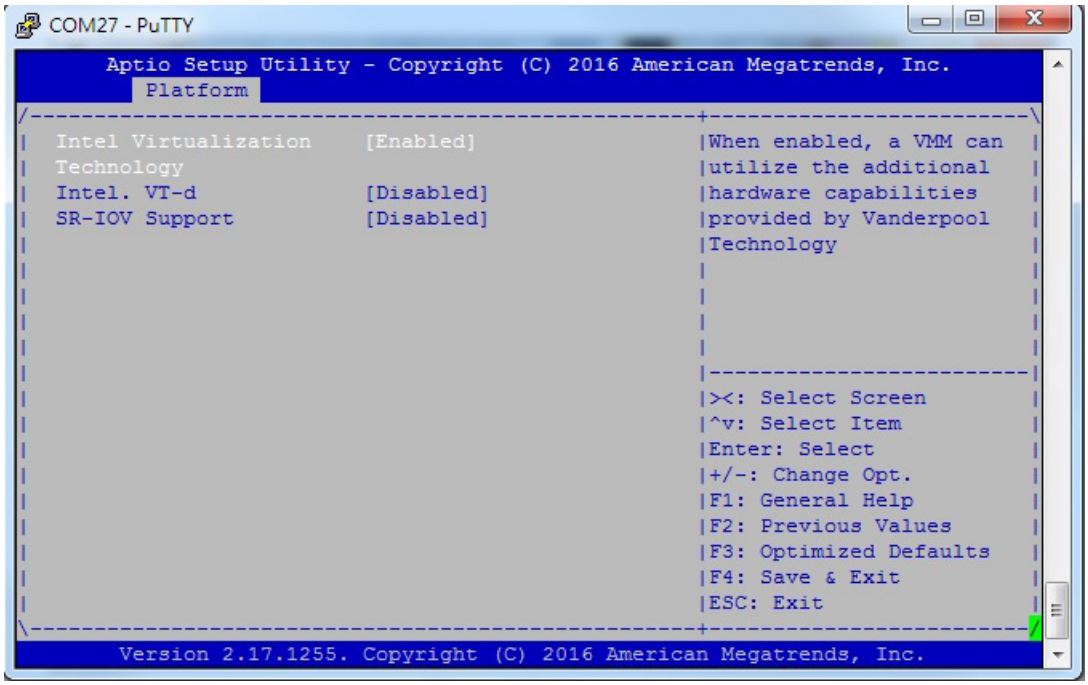


Figure 2.6 Virtualization

Table 2.4: Virtualization

Feature	Options	Description	Help text
Intel Virtualization Technology	Disabled Enabled	Enable or disable BIOS support for the Vanderpool Technology	Enable the Vanderpool Technology, take effect after reboot.
Intel(R) VT-d	Enabled Disabled	Enable or disable Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.	Enable or disable Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.
SR=IOV Support	Enabled Disabled	If system as SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.	If system as SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support

2.2.2.4 Platform Management

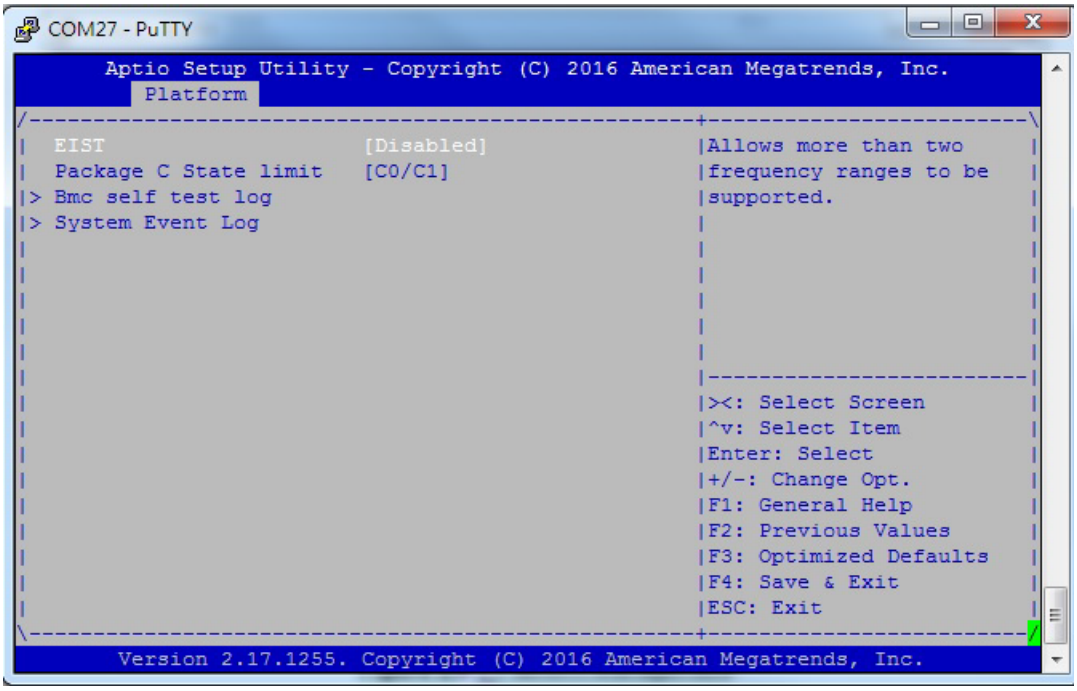


Figure 2.7 Platform Management

Table 2.5: Platform Management

Feature	Options	Description	Help text
EIST	Disabled Enabled	Enable or disable BIOS support for Enhanced Intel SpeedStep Technology	When enabled, OS sets CPU frequency according load. When disabled, CPU frequency is set at max non-turbo.
Turbo Mode	Enabled Disabled	Enable or disable processor Turbo mode.Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available not exceed CPU defined limits.	Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available not exceed CPU defined limits.
Package C State limit	**C0/C1,** C2, C3, C6, C7, C7s, C8, C9, C10, AUTO	Package C State limit.	Package C State limit.

BMC self test log

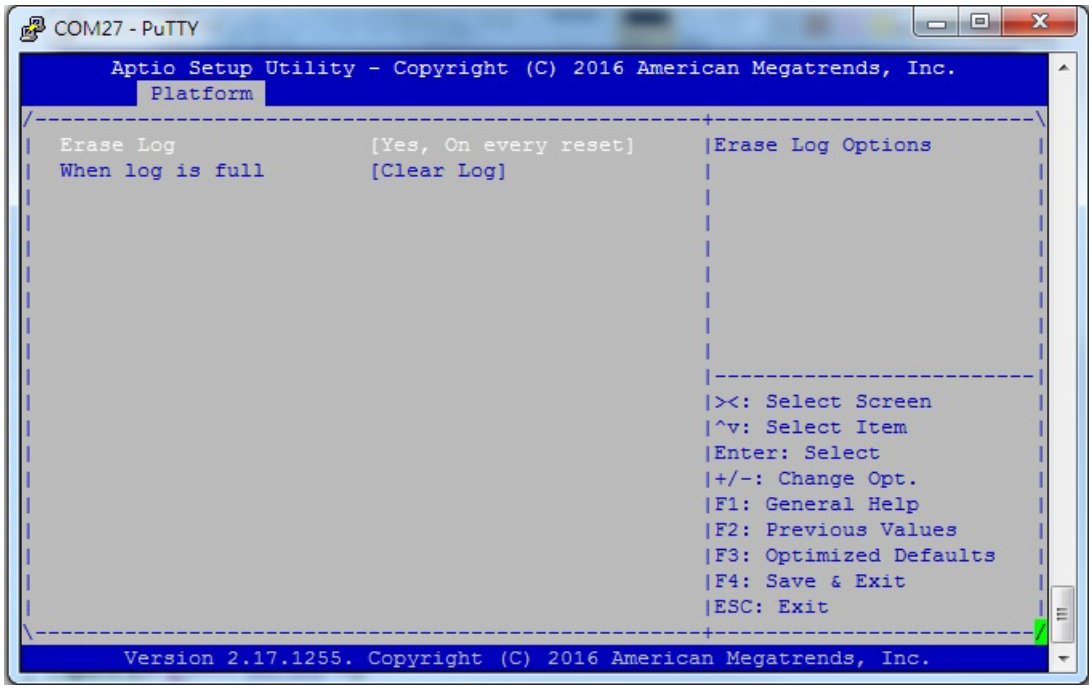


Figure 2.8 BMC self test log

Table 2.6: BMC self test log			
Feature	**Options**	**Description**	**Help text**
Erase Log	**Yes, on every reset** No	Decide if the log should be erased every time the blade resets.	Erase log options
When log is full	**Clear Log** Do not log any more	Select the behavior when the log is full.	Select the action to be taken when the log is full.

System Event log

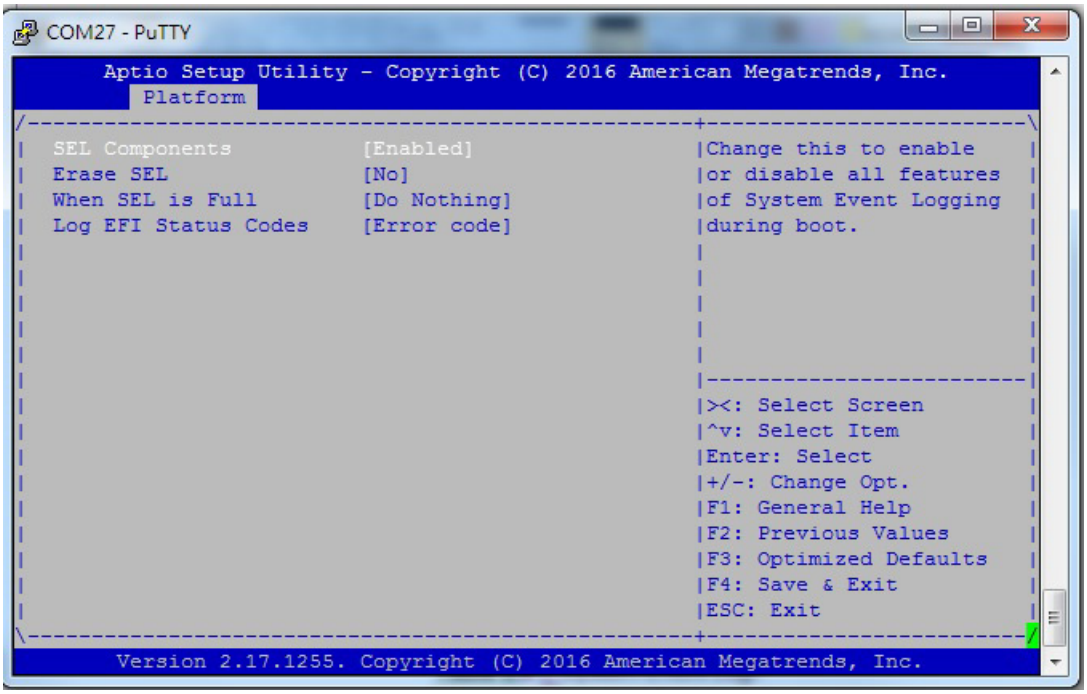


Figure 2.9 System Event Log

Table 2.7: System Event Log

Feature	Options	Description	Help text
SEL components	Enabled Disabled	Change this to enable or disable all the features of System Event Logging during boot.	Change this to enable or disable all the features of System Event Logging during boot.
Erase SEL	No, Yes, On next reset, Yes, On every reset	Choose options for erasing SEL.	Choose options for erasing SEL.
When SEL is Full	Do Nothing, Erase Immediately	Choose options for reactions to a full SEL.	Choose options for erasing SEL.
Log EFI Status Codes	Disabled, Both, Error code, Progress code	Disable the logging of EFI Status Codes or log only error code or only progress code or both.	Disable the logging of EFI Status Codes or log only error code or only progress code or both.

2.2.2.5 Trusted Platform Module

While the TPM is presented (only on the conduction cooled SKU or the XMC SKU), the Trust Computing setting will be configurable in the BIOS.

Table 2.8: Trust computing setting

Feature	Options	Description	Help text
Security Device Support	**Enable** Disabled	The supported Secure Hash Algorithm shows here.	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
SHA-1 PCR Bank	**Enable** Disable	Enable or disable the Platform Configuration Register banks for Secure Hash Algorithm 1	Enable or Disable SHA-1 PCR Bank
SHA256 PCR Bank	**Enable** Disable	Enable or disable the Platform Configuration Register banks for Secure Hash Algorithm 2 with the digests of 256 bits	Enable or Disable SHA256 PCR Bank
Pending operation	**None** TPM Clear	The setting for scheduling the TPM operation.	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	**Enable** Disabled	Platform domain controlled by platformAuth used to protect the integrity of the platform/firmware services.	Enable or Disable Platform Hierarchy

Table 2.8: Trust computing setting			
Storage Hierarchy	**Enable** Disabled	Security domain controlled by ownerAuth used to protect the security of the user.	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	**Enable** Disabled	Privacy domain controlled by endorsementAuth used to expose the identity of the platform/user.	Enable or Disable Endorsement Hierarchy

2.2.3 Hardware Setup

Select the chipset tab from the MIC-6330 setup screen to enter the Hardware setup screen. Users can configure the parameters of CPU configuration, Northbridge, Southbridge, Super IO and HW monitor respectively.

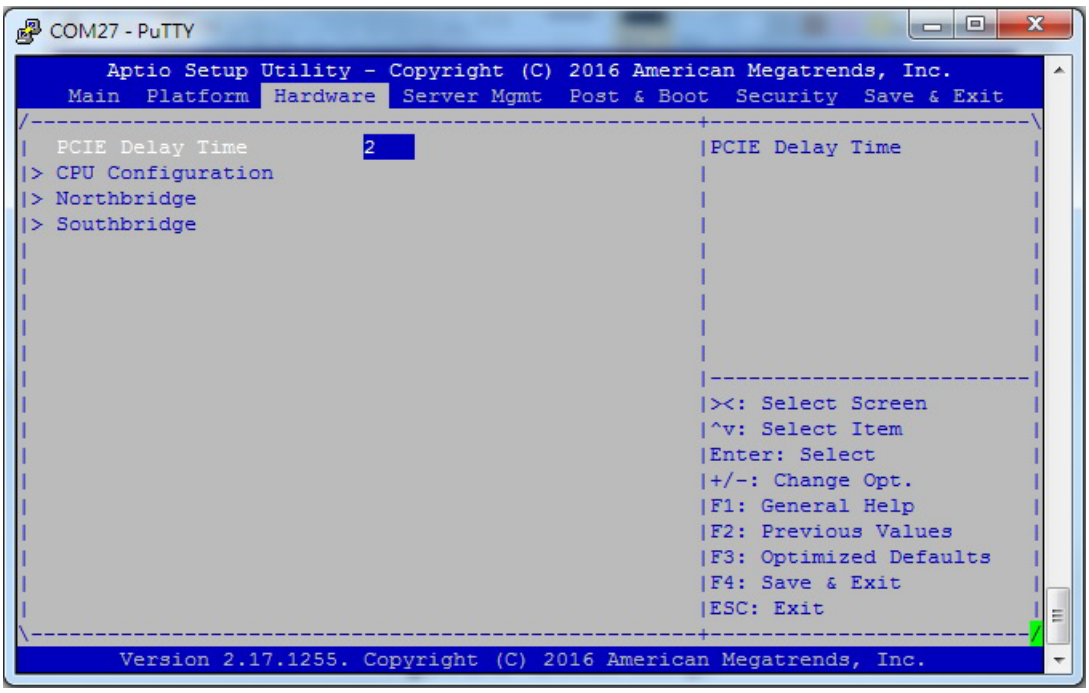


Figure 2.10 Hardware Settings

2.2.3.1 CPU configuration

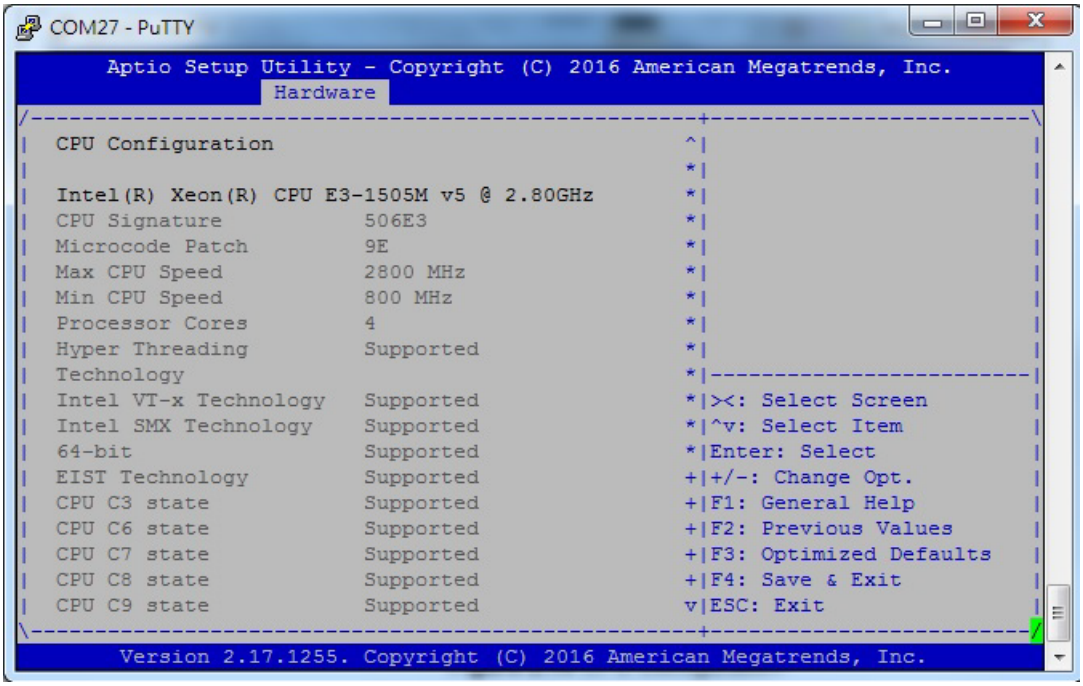


Figure 2.11 CPU Configuration

2.2.3.2 Northbridge

Users can set up all parameters related to the IOH function in the North Bridge page. Moreover, the MIC-6330 BIOS allows users to configure the PCIe link speed (gen1, gen2 or gen3) and its functions visible (x8, x4x4 or x2x2x2x2) in the northbridge configuration submenu.

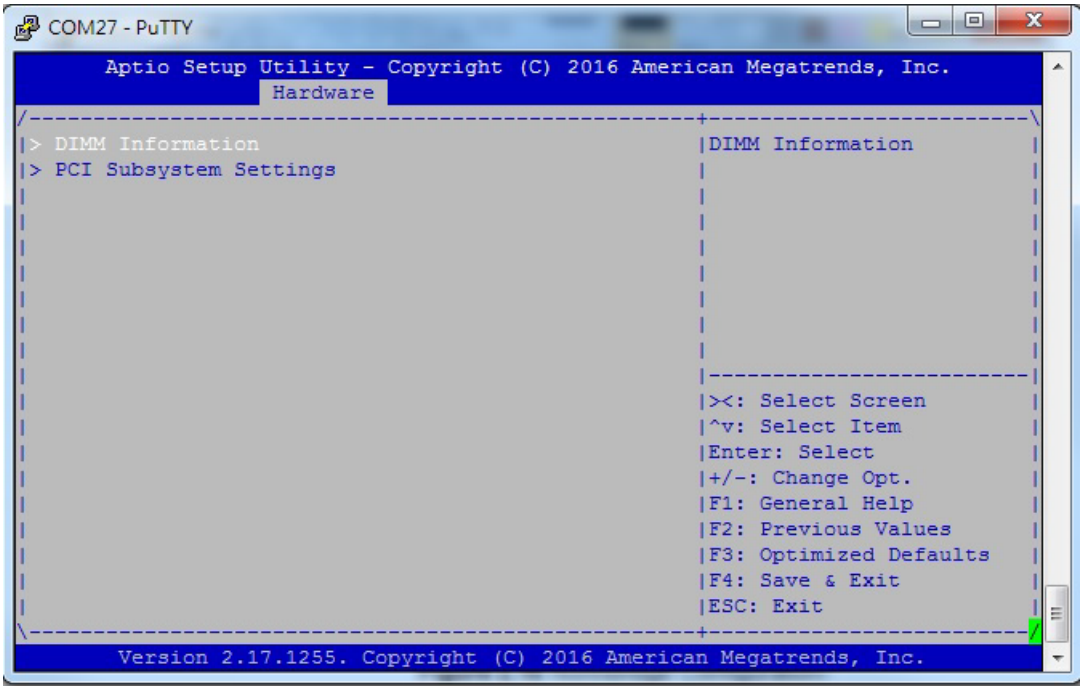


Figure 2.12 Northbridge Configuration

DIMM information

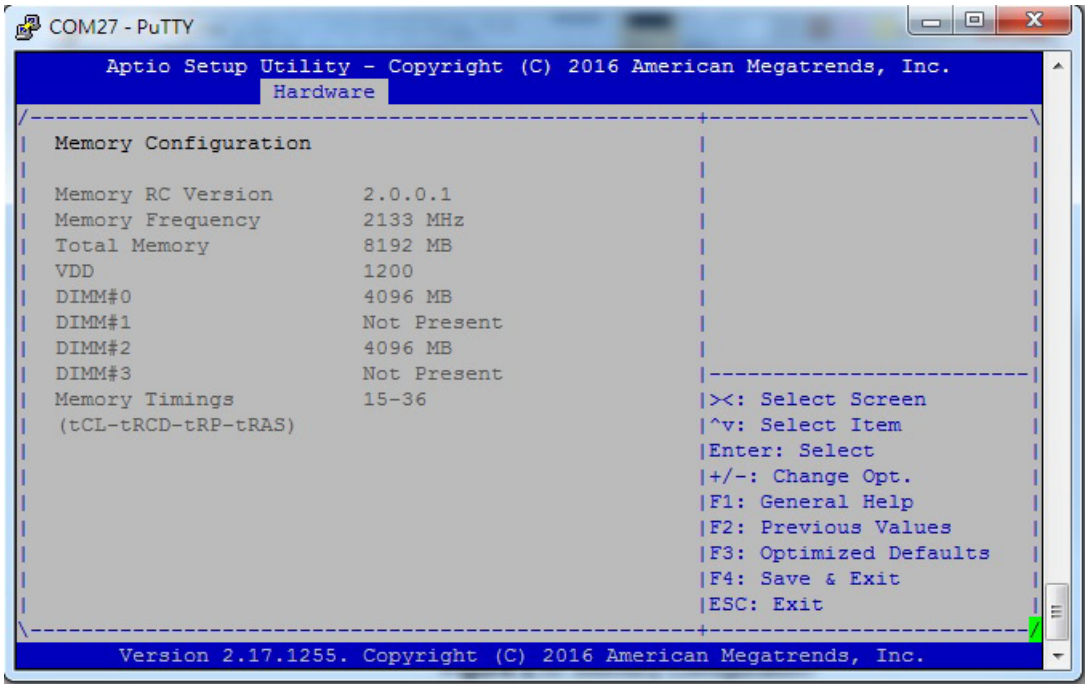


Figure 2.13 Memory Configuration

PCI Subsystem Settings

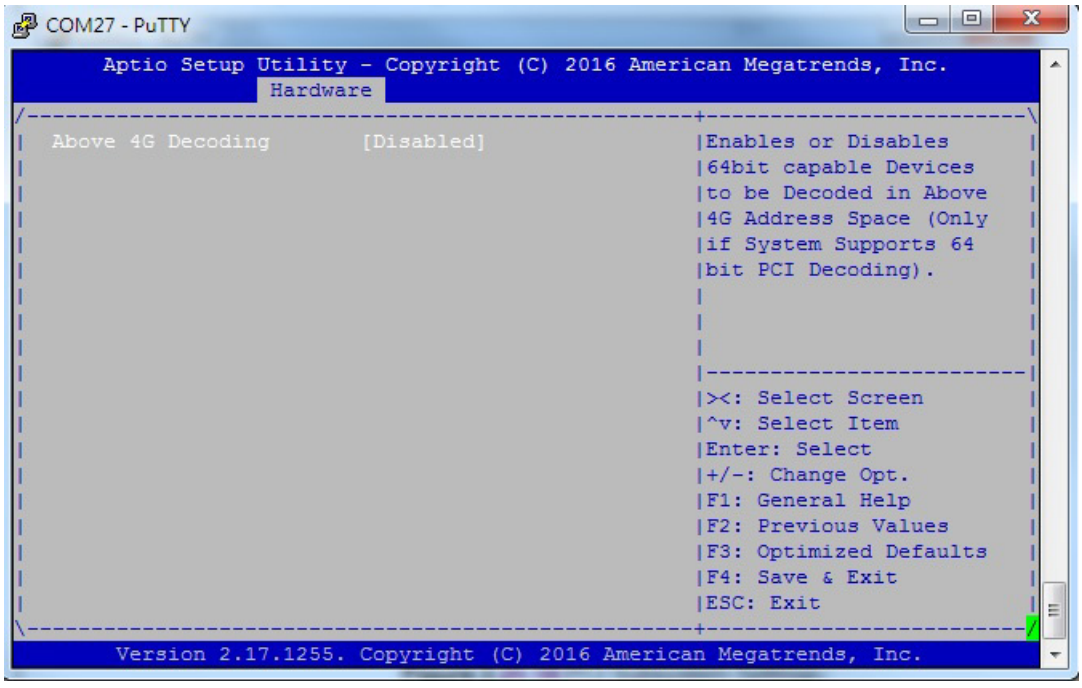


Figure 2.14 PCI Subsystem Settings

Table 2.9: PCI Subsystem Settings			
Feature	**Options**	**Description**	**Help text**
Above 4G Decoding	Disabled Enabled	Enable or disable 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).	Enable or disable 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

2.2.3.3 Southbridge

Users can set up all parameters related to the PCH function in the South Bridge page.

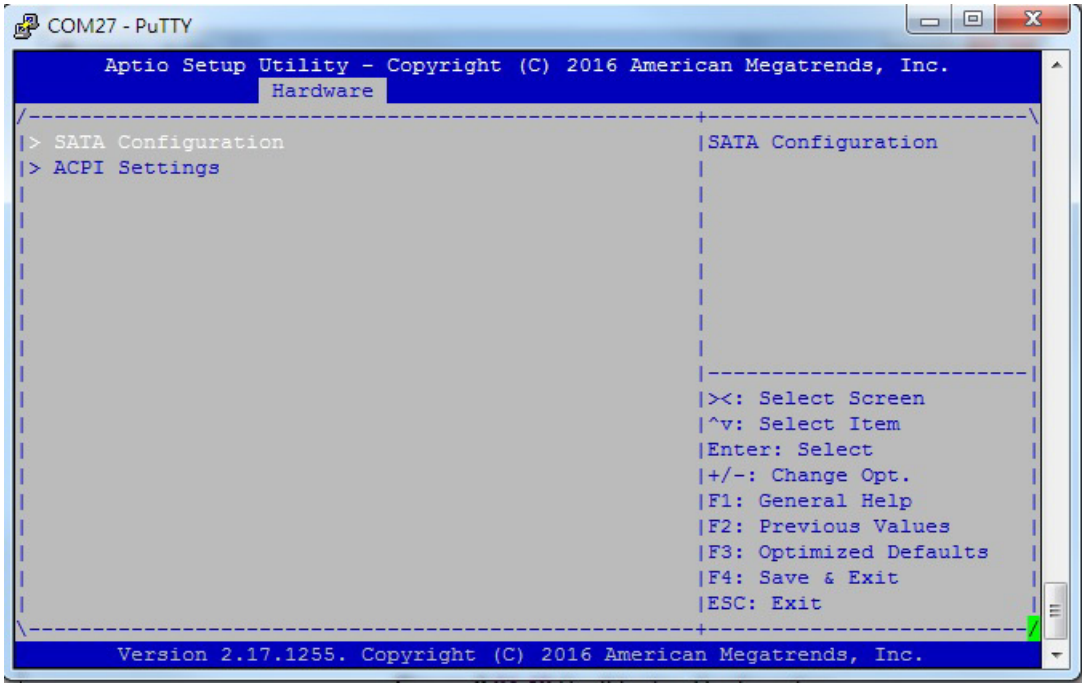


Figure 2.15 Southbridge Configuration

SATA Configuration

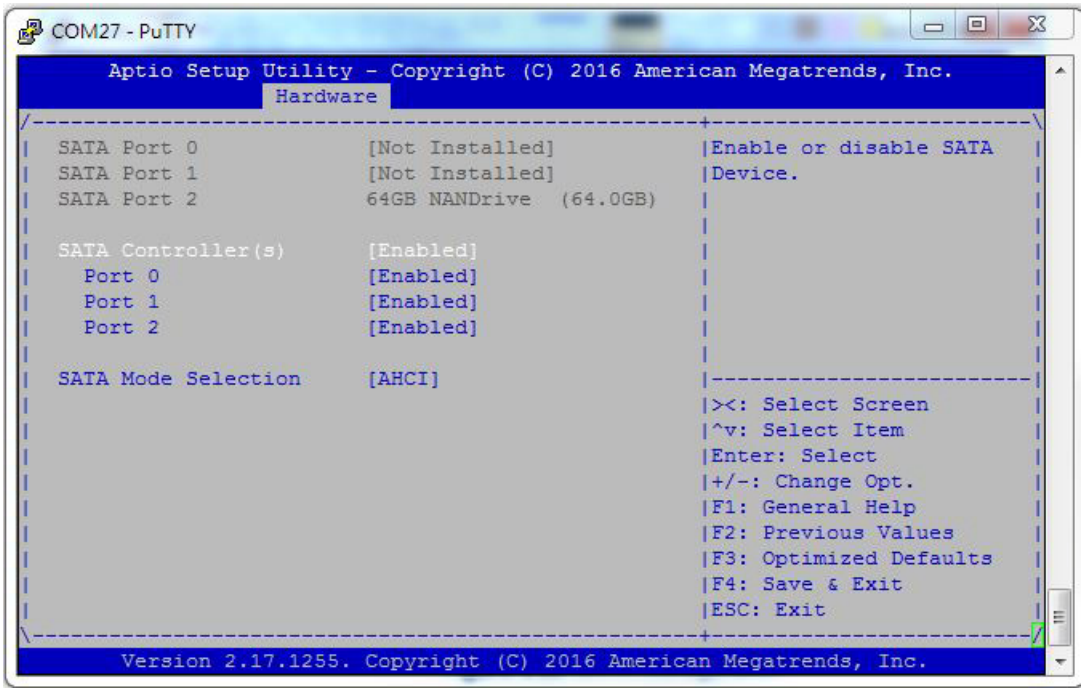


Figure 2.16 SATA Configuration

Table 2.10: SATA Configuration

Feature	Options	Description	Help text
SATA Controller	Disabled Enabled	Enable or disable SATA Controller	Enable or disable SATA Controller
SATA Mode	AHCI IDE	Configure SATA as IDE or AHCI.	This will configure SATA as IDE or AHCI.

ACPI Settings

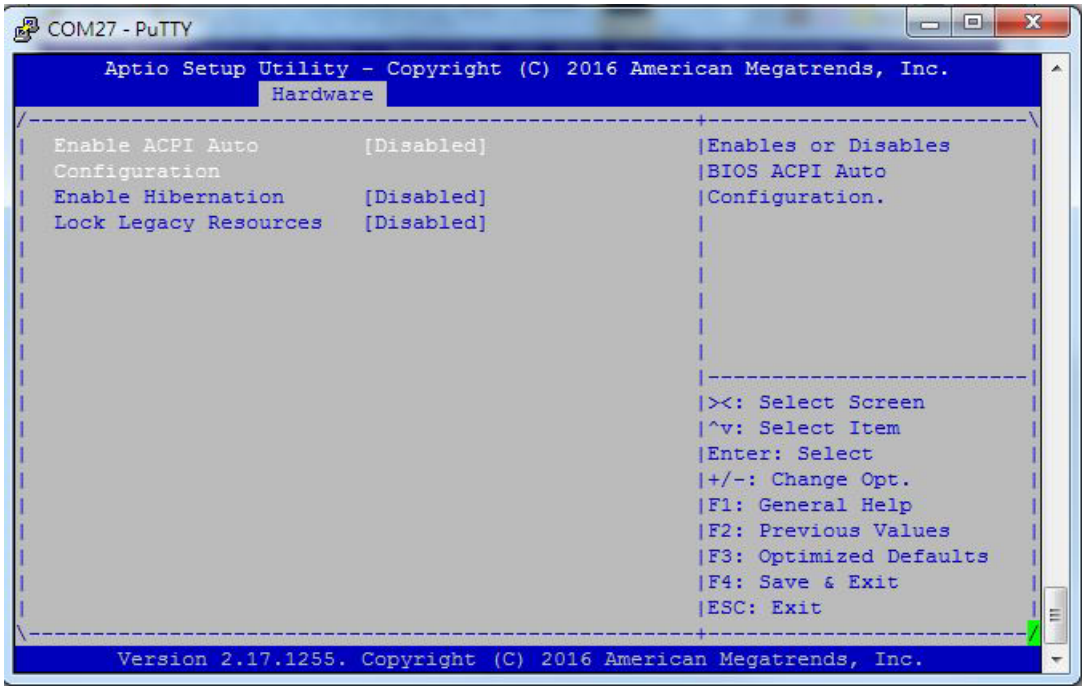


Figure 2.17 ACPI Settings

Table 2.11: ACPI Settings

Feature	Options	Description	Help text
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable BIOS ACPI Auto Configuration.	Enable or disable BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled Enabled	Enable or disable System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.	Enable or disable System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
Lock legacy resources	Disabled Enabled	Enables or Disables Lock of Legacy Resources	Enables or Disables Lock of Legacy Resources

2.2.4 Server Management (Mgmt) Setup

The Server Mgmt menu supports shows BMC related features such as OS Watchdog Timer, etc. For details of the BMC self test log and system event log, users can decide to enable the function to record the logs, erase the logs through BMC self test log submenu, or the system event log submenu.

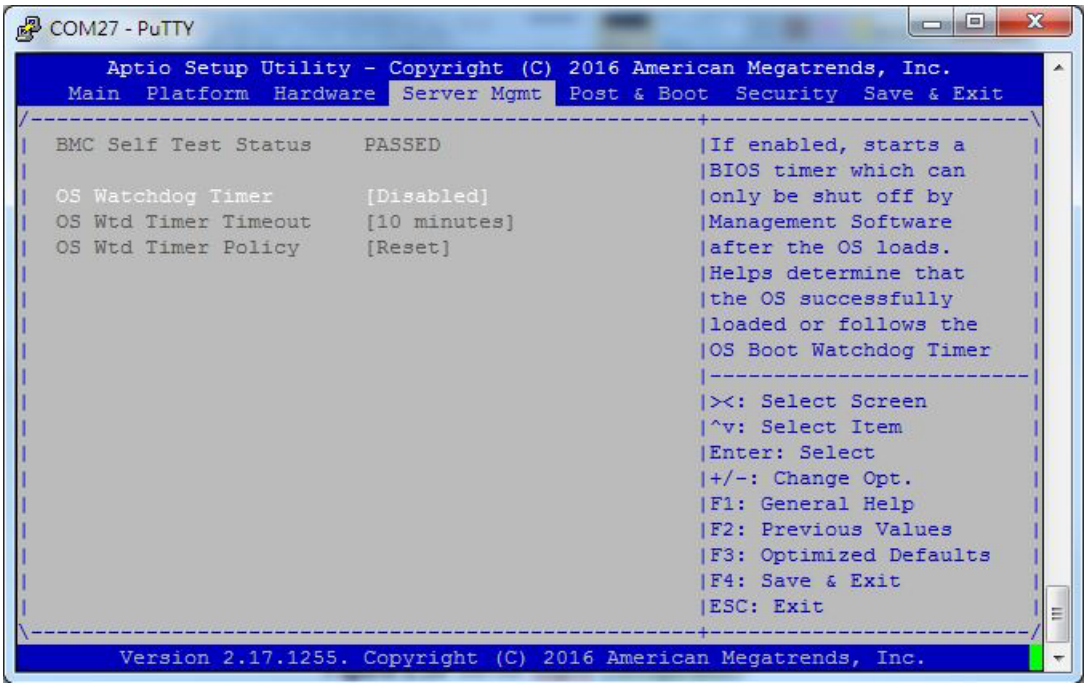


Figure 2.18 Server Mgmt Configuration

2.2.5 Boot Setup

The Post & Boot menu allows configuring POST behavior and boot options.

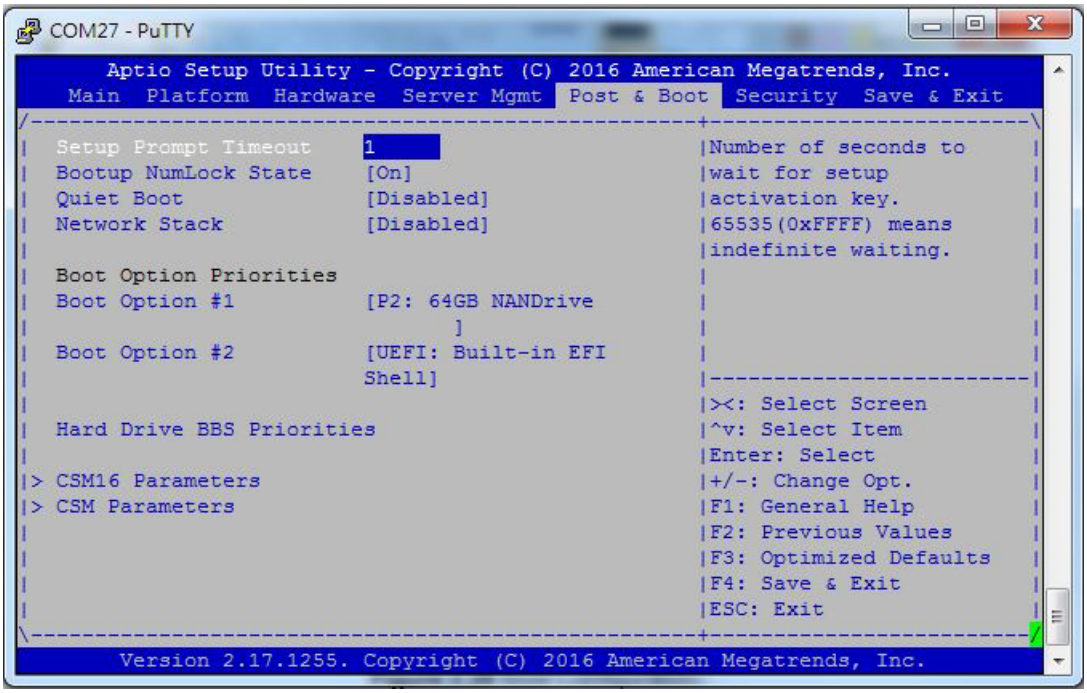


Figure 2.19 Boot Configuration

Table 2.12: SATA Configuration			
Feature	**Options**	**Description**	**Help text**
Setup Prompt Timeout	1 to 65535 1	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	Number of seconds to wait for setup activation key. 65535(0xFFFF) means wait indefinitely.
Bootup Num-Lock State	On Off	Select the keyboard NumLock state.	Select the keyboard NumLock state.
Quiet Boot	Disabled Enabled	If enabled, POST messages are not displayed on console. This might slightly speed up booting. If disabled, POS messages are displayed on console.	Enable or disable Quiet Boot option.
Network Stack	Disabled Enabled	Enable or disable UEFI Network Stack.	Enable or disable UEFI Network Stack.
Boot Option #1 to #N	Type: Boot device	Specify the priority of the available boot sources. The list includes USB flash, SAS Hard Drive, SATA Hard Drive and UEFI Network PXE. Other supported devices may be dynamically added to the list.	Specify the priority of the available boot sources.

Drive types appear in the boot device priority menu even if no drives are present i.e. the drives that are not connected at the moment only have the “Type” information.

Boot Device Priority sub-menu (boot sources) and same number of sub-menus 'xxx Boot Device' are always present even if no device is present in the corresponding boot device sub-menu.

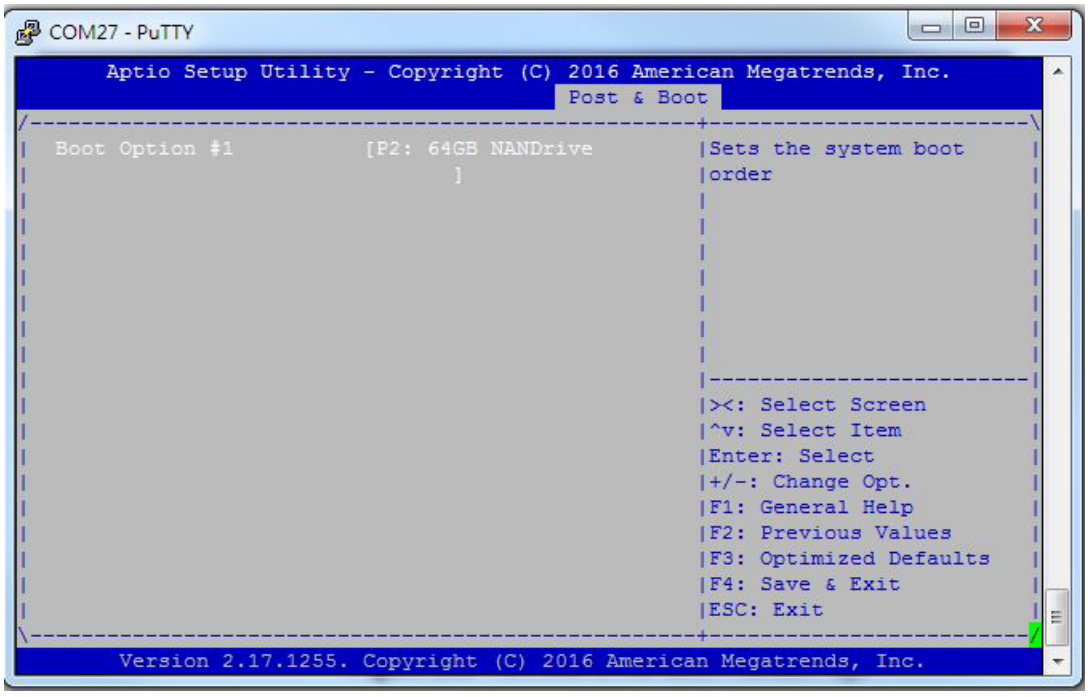


Figure 2.20 Hard Disk Driver BBS Priorities Page

Table 2.13: Hard Disk Driver BBS Priorities Settings			
Feature	**Options**	**Description**	**Help text**
Boot Option #N	N/A	Specify the boot priority of the available devices.	Set the system boot order

2.2.5.1 CSM16 Parameters

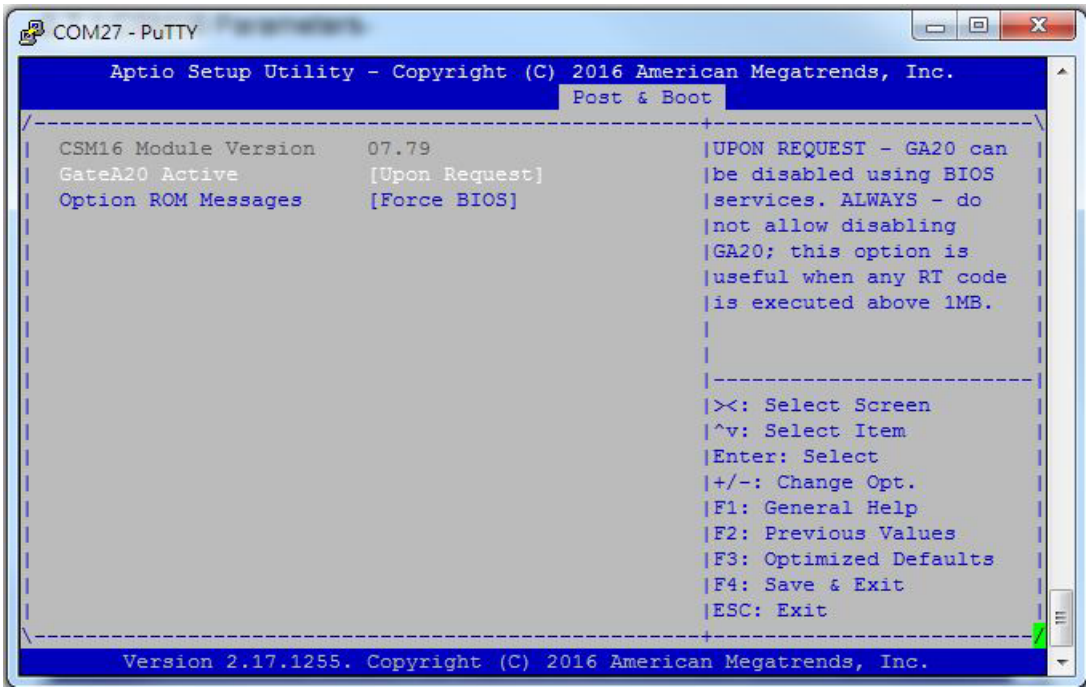


Figure 2.21 CSM16 Parameters

Table 2.14: CSM16 Parameters			
Feature	**Options**	**Description**	**Help text**
GateA20 Active	Upon Request Always	This option can allow or disallow the addressing bus from getting messages from the A20 line.	Upon Request – GA20 can be disabled using BIOS services. Always – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM	Set display mode for Option ROM

2.2.5.2 CSM Parameters

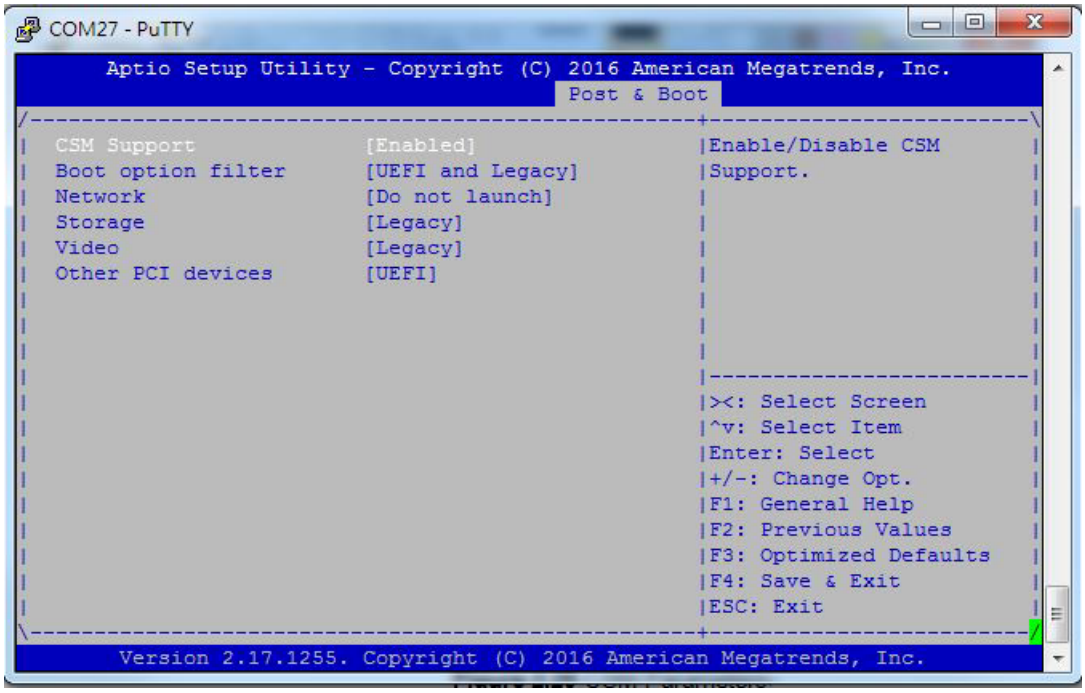


Figure 2.22 CSM Parameters

Table 2.15: CSM Parameters

Feature	Options	Description	Help text
CSM support	Disabled Enabled	Enable/ Disable CSM Support	Enable/ Disable CSM Support
Boot option filter	UEFI and Legacy UEFI only Legacy only	This option controls Legacy/ UEFI ROMs priority	This option controls Legacy/ UEFI ROMs priority
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM	Controls the execution of UEFI and Storage PXE OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM	Controls the execution of UEFI and Legacy Video OpROM
Other PCI devices	**UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video	Determines OpROM execution policy for devices other than Network, Storage, or Video

2.2.6 Security Setup

The Security page allows enabling password protection and entering passwords. Two password levels are provided: Administrator and User. When logging at Administrator level, all configuration parameters can be modified. At User privilege level, certain parameters cannot be changed and certain actions cannot be performed, especially the following options:

- Modify critical platform parameters
- Disable password support
- Modify the administrator password.

Those options are showed in a grey, non-selectable, read-only status at User privilege level.

If Administrator password is enabled, the BIOS will prompt the user for a password before entering the setup menu. If User password is enabled, the BIOS will prompt the user for a password before entering the setup menu and before entering OS. If password protection is disabled, all users have administrator rights.

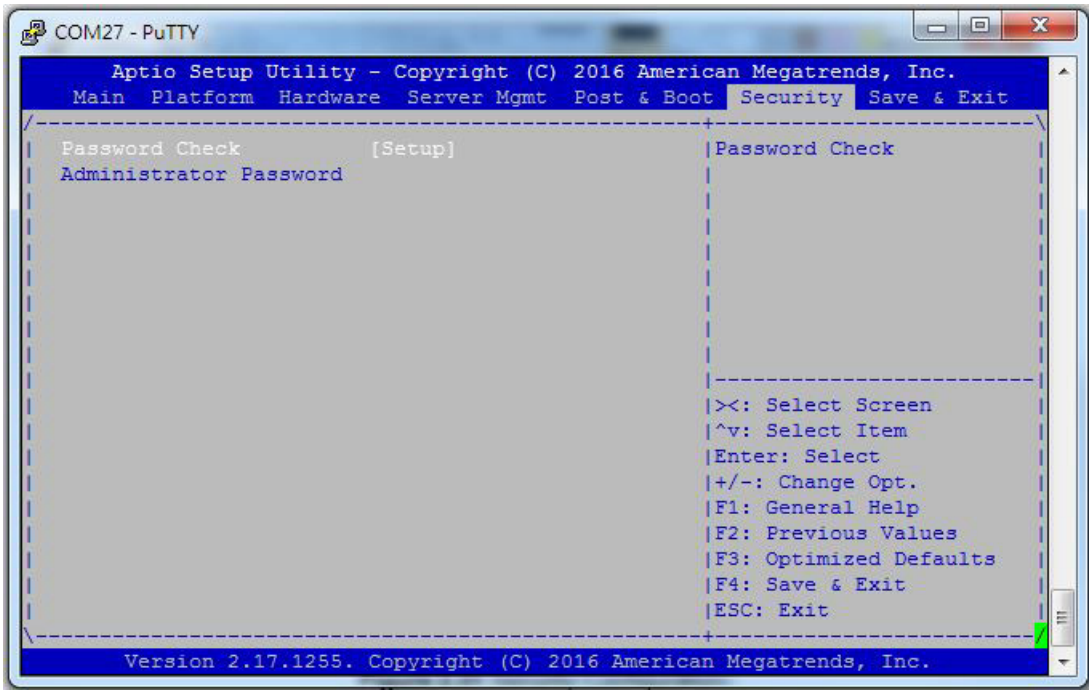


Figure 2.23 Security Configuration

2.2.7 Save & Exit Option

The Save & Exit page provides different options to exit the setup menu and to restore default values for all configuration parameters.

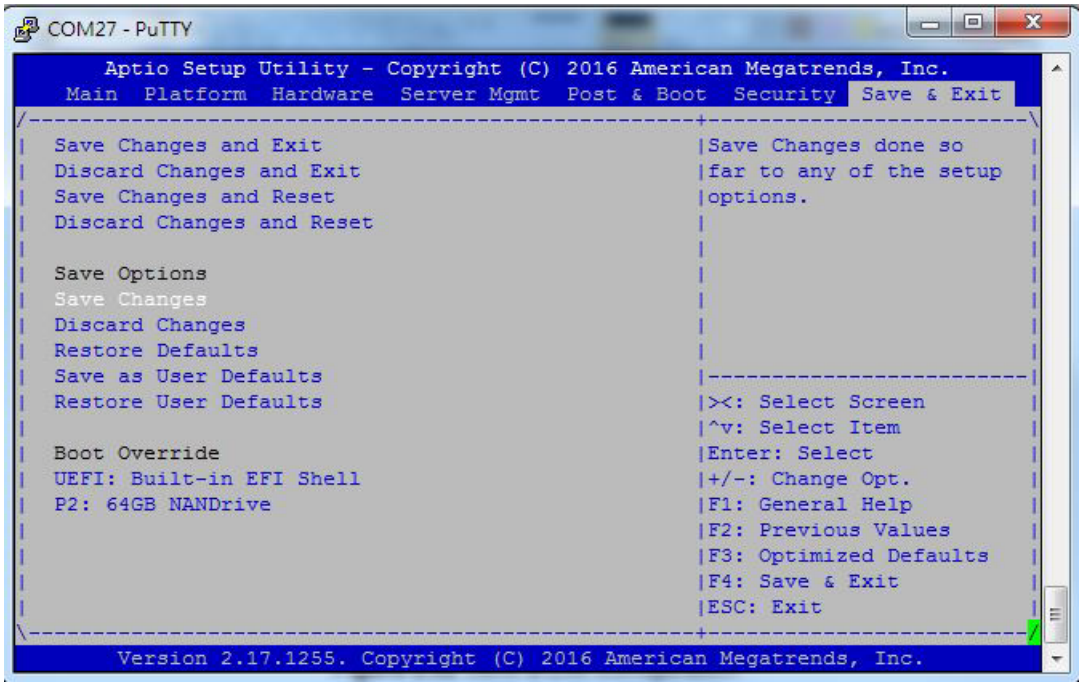


Figure 2.24 Save & Exit Configuration

Table 2.16: Save & Exit Configuration

Feature	Options	Description	Help text
Save Changes and Exit	N/A	Save modified settings into non-volatile memory and reboots the system if need.	Exit system setup after saving the changes.
Discard Changes and Exit	N/A	Discard modified settings, exit setup and continue booting the system with these old values.	Exit system setup without saving any changes.
Save Changes and Reset	N/A	Save modified settings into non-volatile memory and reboots the system.	Reset the system after saving the changes.
Discard Changes and Reset	N/A	Discard modified settings, reverts to the state when setup was entered and reboots with these old values.	Reset system setup without saving any changes.
Save Changes	N/A	Save changes of the setup option which have done so far.	Save Changes done so far to any of the setup options.
Discard Changes	N/A	Discard modifications to settings and reverts to the state when Setup was entered.	Discard Changes done so far to any of the setup options.
Restore Defaults	N/A	Load the factory default settings.	Restore/Load Default values for all the setup options.
Save as User Defaults	N/A	Save the changes done so far as User Defaults.	Save the changes done so far as User Defaults.
Restore User Defaults BIOS	N/A	Restore the User Defaults to all the setup options.	Restore the User Defaults to all the setup options.

Chapter 3

BMC Firmware Operation

This chapter describes the BMC firmware features.

3.1 Module Management

The IPMI Baseboard Management Controller (BMC) located on the MIC-6330 is the essential part of the Board. It acts as standard IPMI management controller. Main tasks are module health (monitoring voltage and temperature sensors), payload state management, information data storage and providing several IPMI communication interfaces.

3.2 IPMI Interfaces

The MIC-6330 provides three main IPMI messaging interfaces to connect to the modules BMC. These are the local IPMB bus (IPMB) for basic communication with other modules in the Chassis, the LAN side band interface (RMCP/RMCP+) and the onboard payload interface to x86 (KCS).

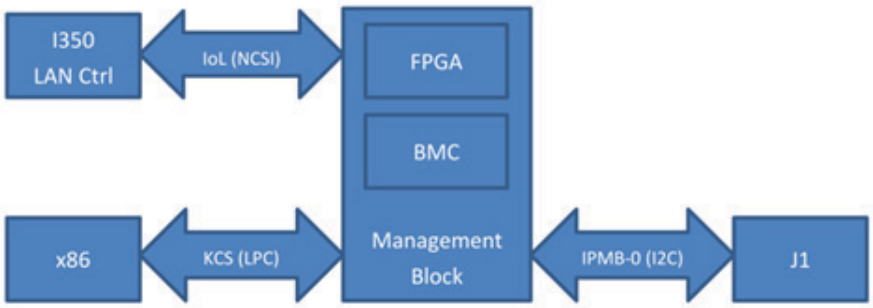


Figure 3.1 IPMI interfaces

3.2.1 IPMB

Basic IPMI connection of a BMC is the I^2C based, serial IPMB interface routed to the Backplane connector. Once plugged in a Backplane and supplied with management power, the BMC discovers the slot connector Geographic Address (GA). The GA is used to assign a unique IPMB address according to the slot number. With this IPMB address, the BMC is able to communicate with other parts in the chassis.

The open source IPMItool can be used to access the BMC via IPMB.

3.2.2 KCS

The Keyboard Controller Style (KCS) protocol is used as IPMI system interface connection to the x86 part on MIC-6330. It's based on the Low Pin Count (LPC) bus and used as the local BMC interface to BIOS and the Operating System (OS) on the Board. KCS is a fast IPMI interface compared to IPMB, but requires active payload.

IPMI driver support is needed to be able to use the IPMItool from OS level via the KCS BMC interface (refer to chapter - Driver and Tools-). With a working IPMI driver, the BMC can be easily accessed from OS via KCS. No interface parameters are needed at all, to use the local onboard IPMI connection:

```
ipmitool <Command>
```

3.2.3 LAN

The IPMI LAN Interface on MIC-6330 is accomplished by using a shared LAN Controller together with the x86 system. In addition to systems PCI-Express link, a LAN controller side-band interface (Network Controller Sideband Interface, short NC-SI) is connected to the BMC. This NC-SI channel is used by the BMC to receive and transmit IPMI management traffic from and to network with help of the LAN controller.

IPMI over LAN (IOL) uses the Remote Management Control Protocol (RMCP, specified in IPMI v1.5) in request-response manner for IPMI communication. IPMI v1.5 LAN messages are encapsulated in RMCP packets, while IPMI v2.0 specification added an enhanced protocol (RMCP+) for transferring IPMI messages and other types of payloads. RMCP+ uses RMCP overall packet format, but defines extensions, such as encryption and the ability to carry additional traffic types (e.g. serial data) in addition to IPMI messages (refer to chapter - Serial over LAN-).

The backplane ports of MIC-6330's Ethernet interfaces can be used for IPMI over LAN.

Following IPMItool parameters are needed to connect to the BMC vial LAN:

```
ipmitool -I lan -H <BMC IP-Address> -U <User> -P <Password> <Command>
```

Command Line Syntax:

-I lan	Specifies Ethernet interface
-H <IP-Address>	IP address assigned to the BMC
-U <User>	User account, default "administrator"
-P <Password>	Password used with specified user account (default password for user "administrator" is "advantech")

3.3 Sensors

Monitoring board voltages and temperatures is one of the main tasks of the BMC populated on the MIC-6330. All important voltages and temperatures are connected to BMC sensors.

Moreover, the BMC Management Subsystem also registers below logical sensors:

- BMC Health sensor
- BMC Watchdog sensor
- FW Progress sensor
- Processer state sensor
- Version change sensor
- System reset sensors
- Advantech OEM Sensor: Integrity Sensor

3.3.1 Sensor list

All sensors available on the MIC-6330 Board are listed in the table below (inclusive FRU Device Locator record):

Table 3.1: Sensor list

No.	Sensor ID	Sensor Type (Event/Reading Type)	Description
0	MIC-6330	-	IPMI FRU Device Locator
1	BMC_HEALTH	Management Subsystem Health (Discrete)	IPMI Management system health sensor
2	VERSION_CHANGE	Version Change (Discrete)	IPMI Version Change sensor
3	BMC_WATCHDOG	Watchdog 2 (Discrete)	IPMI BMC Watchdog sensor
4	PROC_STATE	Processor (Discrete)	IPMI Processer sensor
5	SYSTEM_RESET	System Boot / Restart Initiated (Discrete)	IPMI System Boot/Restart sensor
6	FW_PROGRESS	System Firmware Progress (Discrete)	IPMI FW Progress sensor
7	INTEGRITY	OEM (Discrete)	Advantech OEM Integrity sensor
8	POWER_GOOD	Power Supply (Discrete)	IPMI Power Supply sensor
9	+12-VOL	Voltage (Threshold)	Payload Power voltage 12V
10	VCC_5-VOL	Voltage (Threshold)	Standby Voltage 5V
11	VCC_3_3-VOL	Voltage (Threshold)	Standby Voltage 3.3V
12	BAT_3-VOL	Voltage (Threshold)	Battery voltage 3V
13	MEM_1_2-VOL	Voltage (Threshold)	Memory voltage 1.2V
14	PCH_1_0-VOL	Voltage (Threshold)	PCH Voltage 1V
15	CPU_0_95-VOL	Voltage (Threshold)	CPU voltage 0.95V
16	CPU_VCORE-VOL	Voltage (Threshold)	CPU core voltage 0.9V
17	SYS-TMP	Temperature (Threshold)	System Temperature
18	CPU-TMP	Temperature (Threshold)	CPU Temperature (PECI)
19	LAN-TMP	Temperature (Threshold)	LAN Temperature

3.3.2 Threshold based sensors

According to the IPMI specification, sensor event thresholds are classified as Non-critical, Critical, or Non-recoverable. When different thresholds are reached, different actions may be executed by carrier or shelf manager (e.g. fan speed adjustment for temperature sensor events).

Below table list the six sensor thresholds specified for threshold based sensors in the following sub chapters.

Table 3.2: Threshold descriptions

Threshold	Description
UNR	Upper Non-recoverable
UC	Upper Critical
UNC	Upper Non-critical
LNC	Lower Non-critical
LC	Lower Critical
LNR	Lower Non-recoverable

3.3.2.1 Voltage sensors

All listed voltages listed below are monitored by the BMC and readable via IPMI.

Table 3.3: Voltage sensor list

Sensor Name	Nominal Value	LNR	LCR	LNC	UNC	UCR	UNR
+12-VOL	12	na	11.160	na	na	12.840	na
VCC_5-VOL	5	na	4.65	na	na	5.35	na
VCC_3_3-VOL	3.3	na	3.118	na	na	3.469	na
BAT_3-VOL	3	na	2	na	na	3.3	na
MEM_1_2-VOL	1.2	na	1.08	na	na	1.32	na
PCH_1_0-VOL	1.0	na	0.9	na	na	1.10	na
CPU_0_95-VOL	0.95	na	0.855	na	na	1.045	na
CPU_VCORE-VOL	0.9	na	0	na	na	1.672	na

3.3.2.2 Temperature sensors

The MIC-6330 supports some temperature sensors, either via board populated IC's (e.g. TMP75) or readings from CPU/Chipset interfaces (PECI/SMBus).

Table 3.4: Temperature sensor list

Sensor Name	Value	LNR	LCR	LNC	UNC	UCR	UNR
SYS-TMP	50	na	na	na	85	95	105
CPU-TMP	40	na	na	na	90	100	110
LAN-TMP	40	na	na	na	100	110	120

3.3.3 Discrete Sensors

3.3.3.1 BMC Device Locator

Each BMC provides a PICMG compliant FRU device locator for the subsystem. This record is used to hold location and type information of the BMC.

3.3.3.2 IPMC Health Sensor

The IPMI defined Management Subsystem Health sensor is part of the designs sensor repository with below specified event data format.

Table 3.5: IPMC Health Sensor event data format

Event Direction	Event Data 1	Event Data 2	Event Data 3
[7] = 0b (Assertion) 1b (Deassertion)	[7:4] = Ch (sensor-specific event extension code in byte 2, unspecified byte 3), [3:0]: Specific Offset	[7:0] = Sensor number	FFh (unspecified)

Following IPMC health events can be generated by this sensor:

Table 3.6: IPMC Health Sensor supported events

Sensor Type	Type Code	Specific Offset	Event
Management	28h	01h	Controller access degraded or unavailable
Subsystem Health		04h	Sensor failure (number in Event Data 2)

3.3.3.3 BMC Watchdog Sensor

The BMC Watchdog sensor is supported according to the Watchdog 2 sensor type listed in the IPMI specification.

3.3.3.4 FW Progress Sensor

The BMC SDR contains a FW Progress sensor in order to support logging of the OS boot process. The BMC supports adding and forwarding of SEL entries from the BIOS/OS system firmware progress events by sending ‘Add sel entry’ commands with the matching sensor type to the BMC through the KCS interface.

3.3.3.5 Version Change Sensor

A Version Change sensor is supported according to the IPMI specification.

3.3.3.6 Processor State Sensor

Furthermore, a processor sensor according to the IPMI specification is implemented with support for several CPU related events.

Table 3.7: Processor Sensor event data format

Event Direction	Event Data 1	Event Data 2	Event Data 3
[7] = 0b (Assertion)	[7:6] = 10b (OEM code in Event Data 2), [5:4] = 10b or 00b (event specific, see below) [3:0]: Specific Offset	(see table below)	BIOS POST code, if specific offset = 03h (Hang in POST failure), otherwise FFh (unspecified).

The available events are specified in the table below:

Table 3.8: Processor Sensor supported events

Sensor Type	Type Code	State Offset	Event
Processor	07h	00h	IERR
		01h	Thermal Trip
		03h	FRB2/Hang in POST failure
		0Ah	Processor Automatically Throttled (PROCHOT)
		0Bh	Machine Check Exception (Uncorrectable)
		0Ch	Correctable Machine Check Error

The sensor event data byte 2 holds the CPU source of the above defined events (if distinguishable) as specified below:

Table 3.9: Processor Sensor event data byte 2

Value	Processor Event Source
00h	CPU 0
01h	CPU 1

A FRB2/Hang in POST failure (offset 03h) event will be generated if the BMC Watchdog bits with timer use BIOS FRB2. The current BIOS POST code will be logged in event data 3 for this event in addition (event data byte 1, [7:4] = Ah, OEM code in Event Data 2 and 3).

For all other supported sensor event offsets, the event data 3 will be unused (FFh, unspecified). Thus event data byte 1 will be filled with 8h (OEM code in Event Data 2 and unspecified byte 3) for all events other than 03h.

3.3.3.7 Reset Sensor

The IPMI defined “System Boot / Restart Initiated” sensor is available in the IPMC SDR. This sensor is intended to acknowledge about payload system resets and is asserted with board resets.

The event message for this sensor is filled with following content:

Table 3.10: Reset Sensor event data format

Event Direction	Event Data 1	Event Data 2	Event Data 3
[7] = 0b (Assertion)	[7:4] = Fh (sensor-specific event extension code in byte 2 and byte 3), [3:0]: Specific Offset	FFh or reset cause if specific offset is 07h (see table below)	FFh or channel number if specific offset is 07h

Following event offsets are supported for this System Boot / Restart Initiated sensor:

Table 3.11: Reset Sensor supported events

Sensor Type	Type Code	Specific Offset	Event
System Boot / Restart Initiated	1Dh	00h	Initiated by power up
		01h	Initiated by hard reset
		07h	System Restart (with use of Event Data bytes2 and 3)

Details to the occurred system restart are available in the event data byte 2, bits [3:0] (bits [7:4] are reserved), if event data 1 specific offset is 07h (System Restart). The reset cause is similar as returned by the Get System Restart Cause command.

Table 3.12: Reset Sensor event data byte 2

Event Data 2 [3:0]	Restart Cause
0h	Unknown (system start/restart detected, but cause unknown)
1h	Chassis Control command [required]
3h	Power-up via power push button (front panel handle) [optional]
4h	Watchdog expiration (see watchdog flags) [required]

If the reset cause is watchdog (4h), additional details are located in the BMC Watchdog sensor.

If event data 1 specific offset is 07h (System Restart), the event data byte 3 holds the channel number used to deliver command that generated restart (per Get System Restart Cause command).

3.3.4 Example Sensor Data

The below example shows a MIC-6330 sensor reading list printed with the open source IPMItool:

```
[root@localhost ~]# ipmitool sdr list
BMC_HEALTH       | 01h | ok  | 160.96 |
VERSION_CHANGE   | 02h | ok  | 160.96 |
BMC_WATCHDOG     | 03h | ok  | 160.96 |
PROC_STATE       | 04h | ok  |  3.96 |
SYSTEM_RESET     | 05h | ok  | 160.96 |
FW_PROGRESS      | 06h | ok  | 160.96 |
INTEGRITY        | 07h | ok  | 160.96 |
POWER_GOOD       | 08h | ok  | 160.96 |
+12-VOL          | 09h | ok  | 10.96 | 12.22 Volts
VCC_5-VOL        | 0Ah | ok  | 10.96 | 5.07 Volts
VCC_3_3-VOL      | 0Bh | ok  | 20.96 | 3.37 Volts
BAT_3-VOL        | 0Ch | ok  | 40.96 | 3.19 Volts
MEM_1_2-VOL      | 0Dh | ok  | 32.96 | 1.22 Volts
PCH_1_0-VOL      | 0Eh | ok  | 20.96 | 1.02 Volts
CPU_0_95-VOL     | 0Fh | ok  |  3.96 | 0.96 Volts
CPU_VCORE-VOL    | 10h | ok  |  3.96 | 1.06 Volts
SYS-TMP          | 11h | ok  | 160.96 | 39 degrees C
CPU-TMP          | 12h | ok  |  3.96 | 42 degrees C
LAN-TMP          | 13h | ok  | 160.96 | 45 degrees C
```

```
[root@localhost ~]# ipmitool sdr elist all
MIC-6330         | 00h | ok  | 160.96 | Dynamic MC @ 84h
BMC_HEALTH       | 01h | ok  | 160.96 |
VERSION_CHANGE   | 02h | ok  | 160.96 |
BMC_WATCHDOG     | 03h | ok  | 160.96 |
PROC_STATE       | 04h | ok  |  3.96 |
SYSTEM_RESET     | 05h | ok  | 160.96 |
FW_PROGRESS      | 06h | ok  | 160.96 |
INTEGRITY        | 07h | ok  | 160.96 |
POWER_GOOD       | 08h | ok  | 160.96 |
+12-VOL          | 09h | ok  | 10.96 | 12.22 Volts
VCC_5-VOL        | 0Ah | ok  | 10.96 | 5.07 Volts
VCC_3_3-VOL      | 0Bh | ok  | 20.96 | 3.37 Volts
BAT_3-VOL        | 0Ch | ok  | 40.96 | 3.19 Volts
MEM_1_2-VOL      | 0Dh | ok  | 32.96 | 1.22 Volts
PCH_1_0-VOL      | 0Eh | ok  | 20.96 | 1.02 Volts
CPU_0_95-VOL     | 0Fh | ok  |  3.96 | 0.95 Volts
CPU_VCORE-VOL    | 10h | ok  |  3.96 | 1.06 Volts
SYS-TMP          | 11h | ok  | 160.96 | 39 degrees C
CPU-TMP          | 12h | ok  |  3.96 | 42 degrees C
LAN-TMP          | 13h | ok  | 160.96 | 45 degrees C
```

3.3.5 Integrity sensor

3.3.5.1 Overview

The Advantech Integrity Sensor is an OEM sensor according to the SDR (Sensor Data Record) definitions in the IPMI specification. Its main purpose is to monitor internal firmware states and report events to the operator that would otherwise go unnoticed (hence “integrity sensor”).

Examples for those events are checksum errors, firmware update success/failure, firmware rollbacks.

3.3.5.2 Sensor Characteristics

The Integrity sensor does not support sensor reading, but generates event messages only. These events are stored in the local System Event Log (SEL) and sent to the default event receiver.

The event message contains three bytes of event data. The first byte defines how the event is supposed to be treated: the value of 0xA0 defines that event data 2 and 3 contain OEM data (please verify the IPMI specification for details on OEM sensors).

Event data 2 is used to identify which component the event relates to. This can either be a HPM.1 component, a logical component/feature on the board (for example FRU, RTC) or simply a board specific event.

Event data 3 [7..3] identifies the action or a subcomponent. For example: If the component in byte 2 was a HPM.1 component, it might report if this was an update, a rollback, or boot failure. If the component in byte 2 was “FRU”, it might indicate the subcomponent = area within the FRU that the event relates to.

Event data 3 [2..0] holds the result code. For the HPM.1 example above, it might report that an update or rollback either succeeded or failed. For the FRU example, it might indicate a checksum error.

3.3.5.3 Event Data Byte Definition

The following list provides the exact Integrity sensor event bytes definition.

Table 3.13: Integrity sensor event definitions

Data Byte	[Bit]	Description	Value	Event Data
1	[7:0]	IPMI Header	0xA0	Event data 2 & event data 3 used as OEM data
2	[7:0]	Component	0x00 – 0x07 0x08 – 0xFE 0xFF	HPM.1 component (FW, FPGA, BIOS…) Logical component (FRU, RTC…) Board specific event
3	[7:3]	Action / Subcomponent	b00000 b00001 b00010 b00011 b00100 b00101 b00110 b00111 b01000 b01001 b01010 b01011 b01100 b01101 b01110 b01111… …b11111	Update Recovery/Rollback Manual Rollback Automatic Rollback Activation Flash 0 Boot Flash 1 Boot Common Header Internal Area Chassis Info Area Board Info Area Product Info Area Multi Record Area Time synchronization Graceful Shutdown Not defined yet… Not defined yet
3	[2:0]	Result	b000 b001 b010 b011 b100 b101 b110 b111	Successful Failed Aborted Checksum Error Timeout Initiated Finished Unspecified Error

3.3.5.4 Event Data Translation

The structured definition allows simple translation of each Integrity Sensor event message. Below is an example Integrity Sensor SEL event (0x0A0100). The three event data bytes could be translated in following manner:

Data 1:	0x0A:	Header
Data 2:	0x01:	logical Component (BMC FW)
Data 3:	0x00:	b 0 0 0 0 00 0 0
		Update Successful

The example Integrity Sensor event reports a successful BMC Firmware update.

3.3.5.5 Event Data Table

All event data combinations supported by the BMC Integrity Sensor can be found in following list.

Table 3.14: Integrity sensor's event data table

Component	Action / Subcomponent	Result	Byte 1	Byte2
BMC FW	Update	Successful	0x01	0x00
	Update	Timeout	0x01	0x04
	Update	Aborted	0x01	0x02
	Activation	Failed	0x01	0x21
	Manual Rollback	Initiated	0x01	0x15
	Automatic Rollback	Initiated	0x01	0x1D
	Rollback	Finished	0x01	0x10
	Rollback	Failed	0x01	0x09
	Graceful Shutdown	Timeout	0x01	0x74
FPGA	Update	Successful	0x02	0x00
	Update	Timeout	0x02	0x04
	Update	Aborted	0x02	0x02
	Recovery	Finished	0x02	0x10
BIOS	Update	Successful	0x03	0x00
	Update	Timeout	0x03	0x04
	Update	Aborted	0x03	0x02
	Flash 0 Boot	Failed	0x03	0x29
	Flash 1 Boot	Failed	0x03	0x31

3.3.5.6 Example Event Identification

The Integrity Sensor is listed as the last MIC-6330 sensor (verify below IPMItool example).

```
[root@localhost ~]# ipmitool sdr elist
…
INTEGRITY        | 07h | ok  | 160.96 |
```

As mentioned before, the Integrity Sensor does not provide a sensor reading (disabled), but supports event generation at any time.

Occurred events are stored as records in the System Event Log and can be read out with following IPMItool command:

```
[root@localhost ~]# ipmitool sel elist
…
684 | 07/15/2016 | 18:49:19 | OEM INTEGRITY | OEM Specific | Asserted
…
```

Detailed information to single system events (event data bytes) in the SEL can be displayed with IPMItool “sel get <entry>”.

```
[root@localhost ~]# ipmitool sel get 0x684
SEL Record ID          : 0684
 Record Type           : 02
 Timestamp             : 07/15/2016 18:49:19
 Generator ID          : 008e
 EvM Revision          : 04
 Sensor Type           : OEM
 Sensor Number         : 06
 Event Type            : Sensor-specific Discrete
 Event Direction       : Assertion Event
 Event Data (RAW)      : a00335
 Event Interpretation  : Missing
 Description           : OEM Specific

Sensor ID              : INTEGRITY (0x6)
 Entity ID             : 160.96
 Sensor Type (Discrete): Unknown (0xC0)
```

The “Event Data” field reflects the three needed bytes to identify the occurred Integrity Sensor event.

3.4 FRU Information

The BMC provides IPMI defined Field Replaceable Unit (FRU) information about the Board. The MIC-6330 FRU data include general board information’s such as product name, HW version or serial number. A total of 2 kB non-volatile storage space is reserved for the FRU data. The boards IPMI FRU information can be made accessible via all BMC interfaces and the information can be retrieved at any time.

3.4.1 FRU Information Access Commands

The FRU device IPMI commands are supported by the BMC to read and write the boards FRU information. Correct and board specific FRU data is programmed to each single module in factory. Please be very careful using the regular IPMI FRU write command (avoid if possible). Wrong FRU data content could destroy the payload functionality!

3.4.2 Example FRU Data

The below example shows a default MIC-6330 FRU data excerpt (Board and Product Info areas) using the Linux “IPMItool”:

```
[root@localhost ~]# ipmitool fru
FRU Device Description : Builtin FRU Device (ID 0)
 Board Mfg Date        : Mon Jan  1 00:00:00 1996
 Board Mfg             : Advantech
 Board Product         : MIC-6330
 Board Serial          : AKA1234567
 Board Part Number     : MIC-6330
 Product Manufacturer  : Advantech
 Product Name          : MIC-6330
 Product Part Number   : MIC-6330
 Product Version       : A1 02
 Product Serial        : AKA1234567
```

3.5 OEM commands

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI defined OEM/Group Network Function (NetFn) Codes 2Eh, 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response. Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The MIC-6330 BMC supports following Advantech IPMI OEM commands:

Table 3.15: OEM command overview

Command	LUN	NetFn	CMD
Store Configuration Settings	00h	2Eh	40h
Read Configuration Settings	00h	2Eh	41h
Read Port 80 (BIOS POST Code)	00h	2Eh	80h
Load Default Configuration	00h	2Eh	F2h

3.5.1 IPMItool Raw Command

To be able to use the Advantech OEM commands with the open source IPMItool, users have to employ the "raw" command of IPMItool. Please find below command structure details of the IPMItool raw command.

General raw request:

```
ipmitool raw <netfn> <cmd> [data]
```

Response, if raw <netfn> is 2Eh (OEM/Group):

```
<IANA Enterprise Number> [data]
```

3.5.2 Configuration Setting OEM Commands

The Read and Store Configuration OEM commands can be used to read and change several important board settings. The following sub-chapters describe the needed command details.

3.5.3 Read Port 80 (BIOS POST Code) OEM Command

To be able to read out the actual BIOS boot state via IPMI, the BMC provides an Advantech OEM command to reflect the actual BIOS POST (Port 80) code.

```
ipmitool raw 0x2e 0x80 0x39 0x28 0x00
```

Response:

```
39 28 00 <POST Code>
```

3.5.4 Load Default Configuration OEM Command

Several configurations settings are provided by the BMC. To reset all of them to their default values, a single OEM command is available to perform this with only one IPMI command.

```
ipmitool raw 0x2e 0xF2 0x39 0x28 0x00
```

Response:

```
39 28 00
```

3.5.5 Swap BIOS Bank OEM Command

There are 2 BIOS banks on the board, one for active BIOS and the other one for redundancy. Swap the BIOS bank manually by the OEM command below. Remember that the BIOS bank could be swap only when the payload power is off.

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x03 0x00 0x00
```

Response:

```
39 28 00
```

3.5.6 Graceful Shutdown Timeout OEM Command

BMC will begin to countdown after it receives the graceful shutdown, and force payload power turnoff after timeout. User can set/get the timeout setting by using the OEM command.

Read graceful timeout setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x0e 0x01
```

Response:

```
39 28 00 <timeout>
```

Change graceful timeout setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x0e 0x01 <timeout>
```

Response:

```
39 28 00
```

3.6 ACPI

3.6.1 ACPI Featured Graceful Shutdown

Note! *The payload OS used with MIC-6330 need to support ACPI to benefit from the module graceful shutdown feature!*

If there's a shutdown request (e.g. hot swap front panel handle "open" event or IPMI command), the BMC will initiate the OS shutdown with help of the ACPI Power Button signal routed to the x86 system. The ACPI daemon running on the payload OS will start to shut down the system once it detects the ACPI event. When the OS shutdown is finished, the payload will indicate the achieved sleep state to the BMC.

3.6.2 Graceful Shutdown Timeout

A Graceful Shutdown timeout is implemented for payload operating systems without ACPI support or in case the shutdown process is not finished (no active x86 sleep state).

If the BMC does not get the activated sleep state signal within the timeout value of 60 seconds, it will power off the payload anyway.

3.7 BIOS Failover/redundancy

3.7.1 Overview

The MIC-6330 supports BIOS redundancy handled by the BMC. Two BIOS SPI flashes are populated on the board. This BIOS redundancy mechanism is responsible to manage the flash failover, in case the actual selected BIOS fail to boot.

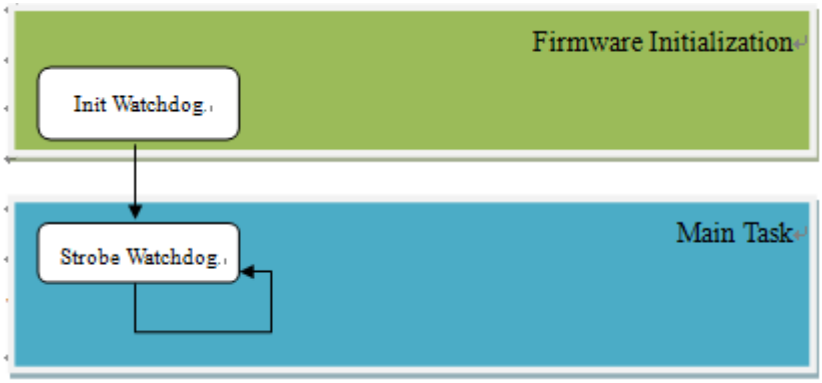
3.7.2 BIOS Boot Watchdog

An IPMI compliant BMC Watchdog, implemented in the BMC, is used to monitor the BIOS boot progress. The BMC will initiate the BIOS SPI flash swap in case of a BMC Watchdog is triggered during BIOS execution (e.g. selected BIOS corrupt).

3.8 Supported Watchdogs

3.8.1 Firmware Watchdog

The FW Watchdog monitors the BMC functionality. If the BMC hangs and stops execution, the watchdog will not be restarted. The watchdog “bites” after a timeout and resets the BMC to recover the controller from current error state.



If the Watchdog is triggered, the IPMB is isolated from the controller. The Payload is not affected and the FRUs operational state stays untouched.

3.8.2 BMC Watchdog

The BMC Watchdog is full IPMI v2.0 Specification compliant. It supports the following IPMI commands:

- Reset Watchdog Timer (IPMI 2.0 Specification 27.5)
- Set Watchdog Timer (IPMI 2.0 Specification 27.6)
- Get Watchdog Timer (IPMI 2.0 Specification 27.7)

To ensure a high reliability of the MIC-6330 Payload, the BMC Watchdog is enabled by default for BIOS monitoring. The details are described in BIOS failover chapter.

3.9 Resets

Several different reset types are support by the board. This chapter provides an overview about the used naming and the differences between the available resets.

3.9.1 Baseboard Management Controller Resets

The MIC-6330 BMC support cold resets following the IPMI specification.

3.9.1.1 BMC Cold Reset

The cold BMC reset causes default setting of all internal and external data/states (e.g. message buffers, interrupt settings, sensor and event configurations, and FRU LED states) and power up defaults to be restored.

Following events lead to BMC cold resets:

- When the BMC is powered on, a cold BMC reset is performed.
- In case management power drops below some critical value, the BMC is cold reset. When the management power returns to its normal value, the BMC is brought out of reset.
- Another example for the cold reset scenario is if the internal watchdog timer of the BMC expires and reset the BMC.

- User can force a BMC cold reset by pressing the front panel reset button for more than five seconds.
- Finally, a cold reset can also be executed by software with help of the standard IPMI “Cold Reset” command.

3.9.2 Payload Reset

In addition to the management controller reset types, the board also support payload resets. The x86 system represents the payload of the MIC-6330 board.

3.9.2.1 Payload Cold Reset

A payload cold reset means hardware reset to the modules payload part, similar to a power on reset. Following events cause payload cold resets:

- Payload power activation after hot swap state change.
- The front panel reset button is pressed for a short period (less than five seconds).
- The PICMG “FRU Control (Cold Reset)” IPMI command is send to the BMC.
- The IPMI Chassis Power command is sent to the BMC
- IPMI BMC Watchdog events.
- Control-Alt-Delete“, also known as the "three-finger salute" (on a connected keyboard).
- Standard operating system reset commands (e.g. Linux “reboot”).

3.10 SOL Setup

Serial over LAN (SOL) is an extension to IPMI over LAN (IOL) and allows to transmit serial data via LAN. It’s defined in the IPMI v2.0 specification and based on the RMCP+ protocol to encapsulate serial data in network packets and exchange them via LAN.

With the help of SOL, user can connect to a virtual serial console (e.g. payload x86 system) from remote. SOL can be used on MIC-6330 for serial-based OS and pre-OS communication over LAN (e.g. OS command-line interface and serial redirected BIOS menu).

3.10.1 Preconditions for SOL

3.10.1.1 Supported LAN Interfaces

All of MIC-6330’s Ethernet interfaces to the backplane can be used for Serial over LAN:

3.10.1.2 Default Parameter

Following default parameters are good to know for the initial MIC-6330 LAN setup:

IP-Address: 192.168.1.1

LAN Channel Number: 5

Username: "administrator"

Password: "advantech"

3.10.2 LAN Configuration with IPMItool

The open source IPMItool utility is used in this chapter for the MIC-6330 SOL and LAN parameter configuration. Any other utility, based on standard IPMI commands, can be used as well.

To get an overview of all possible commands within an IPMItool command group, please use the single keywords (e.g. “lan”, “user” or “sol”) only.

3.10.2.1 LAN Commands

- lan print [channel number]

Get the LAN configuration parameters for a given channel.

```
[root@localhost ~]# ipmitool lan print
Set in Progress         : Set Complete
Auth Type Support       : NONE MD5 PASSWORD
Auth Type Enable        : Callback : NONE MD5 PASSWORD
                        : User     : NONE MD5 PASSWORD
                        : Operator : NONE MD5 PASSWORD
                        : Admin    : NONE MD5 PASSWORD
                        : OEM      :
IP Address Source       : Static Address
IP Address              : 192.168.1.1
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0b:ab:3e:45:87
Default Gateway IP      : 0.0.0.0
RMCP+ Cipher Suites     : 0,1,2,3,6,7,8,11,12
Cipher Suite Priv Max   : aaaaaaaaaXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
                        :     O=OEM
```

- lan set <channel> <command> [option]

This command can be used to change several BMC LAN parameters (e.g. IP address, netmask, gateway IP address,…). Below example demonstrates how to change the BMC IP address.

```
[root@localhost ~]# ipmitool lan set 5 ipaddr 172.21.35.104
Setting LAN IP Address to 172.21.35.104
```

3.10.2.2 User Commands

- user list

Get the list of all supported users.

```
[root@localhost ~]# ipmitool user list
ID  Name             Callin  Link Auth  IPMI Msg   Channel Priv Limit
1                     true    true       true       NO ACCESS
2   callback          true    true       true       NO ACCESS
3   user              true    true       true       NO ACCESS
4   operator          true    true       true       NO ACCESS
```

- user set name <user id> [username]

This command can be used to change the user name.

```
[root@localhost ~]# ipmitool user set name 2 newuser
```

- user set password <user id> [password]

This command can be is used change the user password.

```
[root@localhost ~]# ipmitool user set password 2 newpassword
```

3.10.3 SOL Session with IPMItool

Advantech recommends using IPMItool to successful open a SOL session with MIC-6330. The "lanplus" interface (RMCP+) of IPMItool must be used to be able to change SOL parameters and establish SOL sessions.

Following general IPMItool parameters are needed for RMCP+ and IPMItool "sol" commands:

```
ipmitool -I lanplus -H <BMC IP-Address> -U <User> -P <Password> sol
<SOL-Command>
```

Command Line Syntax:

-I lanplus	Specifies RMCP+ as desired protocol
-H <IP-Address>	IP address assigned to the BMC
-U <User>	User account, default “administrator”
-P <Password>	Password used with specified user account (default password for user “administrator” is “advantech”)

3.10.3.1 SOL Parameter Commands

- sol info [channel number]

Read out the SOL configuration parameters for a given channel.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password> sol
info
Set in progress                 : set-complete
Enabled                         : false
Force Encryption                : true
Force Authentication            : true
Privilege Level                 : ADMINISTRATOR
Character Accumulate Level (ms) : 250
Character Send Threshold        : 32
Retry Count                     : 2
Retry Interval (ms)             : 1000
Volatile Bit Rate (kbps)        : 115.2
Non-Volatile Bit Rate (kbps)    : 115.2
Payload Channel                 : 7 (0x07)
Payload Port                    : 623
```

- sol set <parameter> <value> [channel]

This command allows modifying special SOL configuration parameters.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password> sol
set

SOL set parameters and values:

  set-in-progress             set-complete | set-in-progress | com-
mit-write
  enabled                     true | false
  force-encryption            true | false
  force-authentication        true | false
  privilege-level             user | operator | admin | oem
  character-accumulate-level  <in 5 ms increments>
  character-send-threshold    N
  retry-count                 N
  retry-interval              <in 10 ms increments>
  non-volatile-bit-rate       serial | 9.6 | 19.2 | 38.4 | 57.6 |
115.2
  volatile-bit-rate           serial | 9.6 | 19.2 | 38.4 | 57.6 |
115.2
```

3.10.3.2 SOL Session Activation

Finally, the IPMItool “sol activate” command need to be issued to establish the SOL session to MIC-6330 from remote.

```
# ipmitool -I lanplus <BMC IP-Address> -U <User> -P <Password> sol
activate
[SOL Session operational.  Use ~? for help]
…
~. [terminated ipmitool]
```

To terminate an active IPMItool SOL session, please use the key sequence“~” + “.” (tilde and dot).

Chapter 4

HPM.1 Update

This chapter describes the update of the following software / firmware components:

- BMC Bootloader
- BMC Firmware

4.1 HPM.1 Preconditions

4.1.1 IPMItool

Before upgrading, users need to prepare a HPM.1 capable update utility. Advantech recommends to use the open and verified “IPMItool” (>= version 1.8.10).

In general, any tool compliant to the PICMG HPM.1 R1.0 specification can be used.

4.1.2 Interfaces

HPM.1 provides a way to upgrade firmware via different interfaces

The MIC-6330 supports following IPMI interfaces:

- KCS (local payload interface, active payload and OS support needed)
- IPMB (remote, bridged via Chassis Manager, independent of payload)
- LAN interface (remote, active payload required)

The upgrade procedures in the following chapters are described with the help of KCS, since this is the easiest method. Using LAN or IPMB is similar, only the IPMI-tool interface parameters, which need to be used, are different.

4.2 BMC bootloader Upgrade

4.2.1 Load New BMC Bootloader Image

Type IPMItool HPM.1 upgrade command and select the new BMC bootloader image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6330_bootloader_standard_1.00.img


PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? (y/
n): y
OK

Performing upgrade stage:

--------------------------------------------------------------------
-----------
|ID  | Name            |                      Ver-
sions                              | %   |
|    |                 |      Active      |      Backup        |
File          |     |
|----|-------------|-----------------|-----------------|------------
-----|----|
|   0|6330 BL       |   1.00 00000000 |   0.23 00000000  |   1.00
00000000  |100%|
|    |Upload Time: 00:20          | Image Size:  27,757 bytes
|
--------------------------------------------------------------------
-----------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.2.2 Activate BMC Bootloader

Although the new BMC bootloader is successfully downloaded to the board (called "deferred" version), it needs to be activated or a BMC reset before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:

Waiting firmware activation...OK
```

4.3 BMC Firmware Upgrade

4.3.1 Load New BMC Firmware Image

Type IPMItool HPM.1 upgrade command and select the new BMC firmware image.

```
[root@localhost ~]# ipmitool hpm upgrade
mic6330_bmc_standard_1.00.img


PICMG HPM.1 Upgrade Agent 1.0.9:

Validating firmware image integrity...OK
Performing preparation stage...
Services may be affected during upgrade. Do you wish to continue? (y/
n): y
OK

Performing upgrade stage:

--------------------------------------------------------------------
-----------
|ID  | Name            |                      Ver-
sions                              | %   |
|    |                 |      Active       |      Backup         |
File          |     |
|----|-------------|-----------------|-----------------|------------
-----|----|
|   1|6330 BMC         |   1.00 00000000 |   0.23 00000000  |   1.00
00000000  |100%|
|    |Upload Time: 00:26          | Image Size:  333252 bytes
|
--------------------------------------------------------------------
-----------
(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

4.3.2 Activate BMC Firmware

Although the new BMC FW is successfully downloaded to the board (called “deferred” version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate

PICMG HPM.1 Upgrade Agent 1.0.9:

Waiting firmware activation...OK
```

4.4 Verify Successful Upgrades

To verify successful updates, the IPMItool hpm check command can be used.

```
[root@localhost ~]# ipmitool hpm check

PICMG HPM.1 Upgrade Agent 1.0.9:

-------Target Information-------
Device Id           : 0x88
Device Revision     : 0x81
Product Id          : 0x6330
Manufacturer Id     : 0x2839 (Advantech)


------------------------------------------------------------------------
------
|ID  | Name        |                    Versions
|
|    |             |     Active      |     Backup      |      Deferred
|
------------------------------------------------------------------------
------
|   0|6330 BL      |   1.00 00000000 | ---.-- -------- | ---.-- ----
---- |
|   1|6330 BMC     |   1.00 00000000 |   1.00 00000000 | ---.-- ----
---- |
------------------------------------------------------------------------
------
(*) Component requires Payload Cold Reset
```

After a successful upgrade, the new backup version should be the former active version (if “Backup” versions are supported). And the new “Active” version should be the version of the used upload file.

Appendix A

Pin Assignments

This appendix describes pin assignments.

A.1 P0 Connector

Table A.1: P0 VPX I/O							
	G	F	E	D	C	B	A
1	VS1(+12V)	VS1(+12V)	VS1(+12V)	NC	NC	NC	NC
2	VS1(+12V)	VS1(+12V)	VS1(+12V)	NC	NC	NC	NC
3	VS3(+5V)	VS3(+5V)	VS3(+5V)	NC	VS3(+5V)	VS3(+5V)	VS3(+5V)
4	IPMB0-B_CLK	IPMB0-B_DAT	GND	NC	GND	SYSRESET	Reserved for NVMRO
5	GAP	GA4	GND		GND	IPMB0-A_CLK	IPMB0-A_DAT
6	GA3	GA2	GND		GND	GA1	GA0
7	NC	GND	NC	NC	GND	NC	NC
8	GND	PCIE_REF_CLK-	PCIE_REF_CLK+	GND	NC	NC	GND

A.2 P1 Connector

Table A.2: P1 VPX I/O									
Plug-In Module				**G**	**F**	**E**	**D**	**C**	**B**	**A**
1	Data plane Port1	X8	x4/ 2 x2	NC	GND	PA_TD0-	PA_TD0+	GND	PA_RD0-	PA_RD0+
2				GND	PA_TD1-	PA_TD1+	GND	PA_RD1-	PA_RD1+	GND
3				+VBAT_RIO	GND	PA_TD2-	PA_TD2+	GND	PA_RD2-	PA_RD2+
4				GND	PA_TD3-	PA_TD3+	GND	PA_RD3-	PA_RD3+	GND
5	Data Plane Port2		x4/ 2 x2	SYS_CON#	GND	PB_TD0-	PB_TD0+	GND	PB_RD0-	PB_RD0+
6				GND	PB_TD1-	PB_TD1+	GND	PB_RD1-	PB_RD1+	GND
7				Reserved	GND	PB_TD2-	PB_TD2+	GND	PB_RD2-	PB_RD2+
8				GND	PB_TD3-	PB_TD3+	GND	PB_RD3-	PB_RD3+	GND
9	User Defined			GPIO1	GND	USB3_TX0-	USB3_TX0+	GND	USB3_RX0-	USB3_RX0+
10				GND	USB2_0-	USB2_0+	GND	USB2_1-	USB2_1+	GND
11				GPIO2	GND	MDIB1-	MDIB1+	GND	MDIB0-	MDIB0+
12				GND	MDIB3-	MDIB3+	GND	MDIB2-	MDIB2+	GND
13	User Defined			GPIO3	GND	MDIA1-	MDIA1+	GND	MDIA0-	MDIA0+
14				GND	MDIA3-	MDIA3+	GND	MDIA2-	MDIA2+	GND
15	Control Plane			Reserved for Mask-able Reset	GND	CPutp02-TD-	CPutp02-TD+	GND	CPutp02-RD-	CPutp02-RD+
16				GND	CPutp01-TD-	CPutp01-TD+	GND	CPutp01-RD-	CPutp01-RD+	GND

Note! *NC: No Connection*

#: Active Low

A.3 P2 Connector

There are two P2 pin definitions. One is for the users who use the 2nd Displayport with two extra TTL COM support, which is applied on MIC-6330-A1A4E & MIC-6330-A1C4E, and the other is for the users who use X8D to the backplane. If you want to use the X8D pins, please contact your local Advantech agency or salesperson for the availability.

Table A.3: 2nd Displayport & TTL UART pin map

	G	F	E	D	C	B	A
1	**GPIO**	GND	SATA0_TX-	SATA0_TX+	GND	SATA0_RX-	SATA0_RX+
2	GND	SATA1_TX-	SATA1_TX+	GND	SATA1_RX-	SATA1_RX+	GND
3	**GPIO**	GND	USB2_2-	USB2_2+	GND	USB2_3-	USB2_3+
4	GND	COM1_DCD	COM1_RI	GND	COM1_RX	COM1_TX	GND
5	**GPIO**	GND	COM1_RTS	COM1_CTS	GND	COM1_DTR	COM1_DSR
6	GND	COM2_DCD	COM2_RI	GND	COM2_RX	COM2_TX	GND
7	**GPIO**	GND	COM2_RTS	COM2_CTS	GND	COM2_DTR	COM2_DSR
8	GND	DP1_SMCLK	DP1_SMDAT	GND	DP1_AUX-	DP1_AUX+	GND
9	**DP1_HPD**	GND	DP1_TX0-	DP1_TX0+	GND	DP1_TX1-	DP1_TX1+
10	GND	DP1_TX2-	DP1_TX2+	GND	DP1_TX3-	DP1_TX3+	GND
11	**HDA_SDO**	GND	HDA_SDIN	HDA_RST	GND	HDA_SYNC	HDA_CLK
12	GND	DP2_SCLK	DP2_SDAT	GND	DP2_AUX-	DP2_AUX+	GND
13	**DP2_HPD**	GND	COM3-CTS	COM3-RTS	GND	COM3-RX	COM3-TX
14	GND	COM4-RTS	COM4-CTS	GND	COM4-RX	COM4-TX	GND
15	**PLTRST#**	GND	DP2_TX0-	DP2_TX0+	GND	DP2_TX3-	DP2_TX3+
16	GND	DP2_TX2-	DP2_TX2+	GND	DP2_TX1-	DP2_TX1+	GND

Note! *NC: No Connection*

#: Active Low

Table A.4: X8D pin map							
	G	F	E	D	C	B	A
1	**GPIO4**	GND	SATA0_TX-	SATA0_TX+	GND	SATA0_RX-	SATA0_RX+
2	GND	SATA1_TX-	SATA1_TX+	GND	SATA1_RX-	SATA1_RX+	GND
3	**GPIO5**	GND	USB2_2-	USB2_2+	GND	USB2_3-	USB2_3+
4	GND	COM1_DCD	COM1_RI	GND	COM1_RX	COM1_TX	GND
5	**GPIO6**	GND	COM1_RTS	COM1_CTS	GND	COM1_DTR	COM1_DSR
6	GND	COM2_DCD	COM2_RI	GND	COM2_RX	COM2_TX	GND
7	**GPIO7**	GND	COM2_RTS	COM2_CTS	GND	COM2_DTR	COM2_DSR
8	GND	DP1_SMCLK	DP1_SMDAT	GND	DP1_AUX-	DP1_AUX+	GND
9	**DP1_HPD**	GND	DP1_TX0-	DP1_TX0+	GND	DP1_TX1-	DP1_TX1+
10	GND	DP1_TX2-	DP1_TX2+	GND	DP1_TX3-	DP1_TX3+	GND
11	**HDA_SDO**	GND	HDA_SDIN	HDA_RST	GND	HDA_SYNC	HDA_CLK
12	GND	DP2_SCLK	DP2_SDAT	GND	DP2_AUX-	DP2_AUX+	GND
13	**DP2_HPD**	GND	Jn6-A1	Jn6-B1	GND	Jn6-D1	Jn6-E1
14	GND	Jn6-A3	Jn6-B3	GND	Jn6-D3	Jn6-E3	GND
15	**PLTRST#**	GND	Jn6-A11	Jn6-B11 +	GND	Jn6-D11	Jn6-E11
16	GND	Jn6-A13	Jn6-B13	GND	Jn6-D13	Jn6-E13	GND

Note! *NC: No Connection*

#: Active Low

COM3 and COM4 is TTL; For XMC X8D, there is no COM3, COM4 or the other DP port available on P2.

A.4 Other Connector

Table A.5: J5 XMC Connector

Pin	A	B	C	D	E	F
1	PETX_P0	PETX_N0	+3.3V	PETX_P1	PETX_N1	VPWR(+5V)
2	GND	GND	NC(JRST#)	GND	GND	PRST#
3	PETX_P2	PETX_N2	+3.3V	PETX_P3	PETX_N3	VPWR(+5V)
4	GND	GND	NC(JTCK)	GND	GND	NC(MRSTO#)
5	PETX_P4	PETX_N4	+3.3V	PETX_P5	PETX_N5	VPWR(+5V)
6	GND	GND	NC(JTMS)	GND	GND	+12V
7	PETX_P6	PETX_N6	+3.3V	PETX_P7	PETX_N7	VPWR(+5V)
8	GND	GND	NC(JTDI)	GND	GND	NC
9	NC	NC	NC	NC	NC	VPWR(+5V)
10	GND	GND	NC(JTDO)	GND	GND	GA0
11	PERX_P0	PERX_N0	NC(MBIST#)	PERX_P1	PERX_N1	VPWR(+5V)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERX_P2	PERX_N2	NC(+3.3V_AUX)	PERX_P3	PERX_N3	VPWR(+5V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PERX_P4	PERX_N4	NC	PERX_P5	PERX_N5	VPWR(+5V)
16	GND	GND	NC(MVMRO)	GND	GND	TBD_SCLK
17	PERX_P6	PERX_N6	NC	PERX_P7	PERX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100Mhz	CLK_100Mhz#	FPGAIO2	NC(WAKE#)	NC(ROOT#)	NC

Table A.6: J6 XMC Connector

Pin	A	B	C	D	E	F
1	J6-A1	J6-B1		J6-D1	J6-E1	
2	GND	GND		GND	GND	
3	J6-A3	J6-B3		J6-D3	J6-E3	
4	GND	GND		GND	GND	
5						
6						
7						
8						
9						
10	GND	GND		GND	GND	
11	J6-A11	J6-B11		J6-D11	J6-E11	
12	GND	GND		GND	GND	
13	J6-A13	J6-B13		J6-D13	J6-E13	
14	GND	GND		GND	GND	
15						
16						
17						

18						
19						

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

B.1 Watchdog Timer Programming Procedure

To program the watchdog timer, you must execute a program that writes a value to I/O port address 443/444 (hex), to Enable/Disable. This output value represents a time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is 1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
. .	
3F	63 sec

After data entry, your program must refresh the watchdog timer by rewriting the I/O port 443 and 443 (hex) while simultaneously setting it. When you want to disable the watchdog timer, your program should read I/O port 444 (hex). The following example shows how you might program the watchdog timer in BASIC:

```
10 REM Watchdog timer example program
20 OUT &H443, data REM Start and restart the watchdog
30 GOSUB 1000 REM Your application task #1,
40 OUT &H443, data REM Reset the timer
50 GOSUB 2000 REM Your application task #2,
60 OUT &H443, data REM Reset the timer
70 X=INP (&H444) REM, Disable the watchdog timer
80 END
1000 REM Subroutine #1, your application task
.
1070 RETURN
2000 REM Subroutine #2, your application task
.
2090 RETURN
```

Appendix C

IO Controller List

C.1 IO Controller List

Table C.1: IO Controller List

IO port	Controller
Displayport to backplane	Intel E3-1505Lv5
VGA	Intel CM236
Onboard flash	Intel CM236
SATA	Intel CM236
SATA to backplane	Intel CM236
USB 2.0/3.0 to front panel	Intel CM236
USB 2.0/3.0 to backplane	Intel CM236
Front Panel RJ45	Intel I210
SERDES to backplane	Intel I350AM4
GBE to backplane	Intel I350AM4
UART to backplane	Lattice LCMXO2 Aspeed AST1010

Appendix D

Glossary

D.1 Glossary

ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
CPU	Central Processing Unit
CPCI	CompactPCI
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
FCBGA	Flip Chip BGA
HDD	Hard Disk Drive
HW	HardWare
I/O	Input/Output
IC	Integrated Circuit
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
MAC	Medium Access Control
OS	Operating System
PCB	Printed Wiring Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical layer Interface
RIO	Rear Input/Output
RS-232	An Interface specified by Electronic Industries Alliance
RTC	Real Time Clock
RTM	Rear Transition Module
SBC	Single Board Computer
SFP	Small Form-factor Pluggable
SPD	Serial Presence Detect
SW	SoftWare
ULV	Ultra Low Voltage
FRU	Field Replaceable Unit
FPGA	Field Programmable Gate Arrays
GbE	Gigabit Ethernet
HPM	Hardware Platform Management
IOL	IPMI-Over-LAN
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
NCSI	Network Controller Sideband Interface
NVRAM	Non-Volatile Random-Access Memory
PCH	Platform Controller Hub

PICMG	PCI Industrial Computer Manufacturers Group
PXE	Pre-boot Execution Environment
RMCP	Remote Management Control Protocol
SDR	Sensor Data Record
SerDes	Serializer/Deserializer
SOL	Serial-Over-LAN
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

Appendix E

BIOS Checkpoint

E.1 BIOS Checkpoint

A status code is a data value used to indicate progress during the boot phase. A subset of these status codes, known commonly as checkpoints, indicates common phases of the BIOS boot process.

Checkpoints are typically output to I/O port 80h, but the Aptio 4.x core can be configured to send status codes to a variety of sources. The Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

While performing the functions of the traditional BIOS, the Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization
- Driver Execution Environment (DXE) – main hardware initialization
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Table E.1: Checkpoint Ranges / Descriptions

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

E.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading

0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	**Description**
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started

0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded

0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	**Description**
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization

0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Appendix F

IPMI/PICMG Command Subset Supported by BMC

F.1 Standard IPMI Commands (v2.0)

F.1.1 IPM Device “Global” Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Device ID	20.1	App	01h	Mandatory	Yes
Cold Reset	20.2	App	02h	Optional	Yes
Warm Reset	20.3	App	03h	Optional	Yes
Get Self Test Results	20.4	App	04h	Mandatory	Yes
Manufacturing Test On	20.5	App	05h	Optional	No
Set ACPI Power State	20.6	App	06h	Optional	No
Get ACPI Power State	20.7	App	07h	Optional	No
Get Device GUID	20.8	App	08h	Optional	Yes
Broadcast ‘Get Device ID’	20.9	App	01h	Optional/Man-datory	Yes

F.1.2 BMC Watchdog Timer Commands

Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Reset Watchdog Timer	27.5	App	22h	Mandatory	Yes
Set Watchdog Timer	27.6	App	24h	Mandatory	Yes
Get Watchdog Timer	27.7	App	25h	Mandatory	Yes

F.1.3 BMC Device and Messaging Commands

Command	**IPMI v2.0 Ref.**	**NetFn**	**CMD**	**IPMI BMC Req.**	**Advantech BMC support**
Set BMC Global Enables	22.1	App	2Eh	Mandatory	Yes
Get BMC Global Enables	22.2	App	2Fh	Mandatory	Yes
Clear Message Flags	22.3	App	30h	Mandatory	Yes
Get Message Flags	22.4	App	31h	Mandatory	Yes
Enable Message Channel Receive	22.5	App	32h	Optional	No
Get Message	22.6	App	33h	Mandatory	Yes
Send Message	22.7	App	34h	Mandatory	Yes
Read Event Message Buf-fer	22.8	App	35h	Optional	Yes
Get BT Interface Capabili-ties	22.10	App	36h	Mandatory	No
Get System GUID	22.14	App	37h	Optional	Yes
Get Channel Authentica-tion Capabilities	22.13	App	38h	Optional	Yes
Get Session Challenge	22.15	App	39h	Optional	Yes
Activate Session	22.17	App	3Ah	Optional	Yes

Set Session Privilege Level	22.18	App	3Bh	Optional	Yes
Close Session	22.19	App	3Ch	Optional	Yes
Get Session Info	22.20	App	3Dh	Optional	Yes
Get AuthCode	22.21	App	3Fh	Optional	No
Set Channel Access	22.22	App	40h	Optional	Yes
Get Channel Access	22.23	App	41h	Optional	Yes
Get Channel Info	22.24	App	42h	Optional	Yes
Set User Access	22.26	App	43h	Optional	Yes
Get User Access	22.27	App	44h	Optional	Yes
Set User Name	22.28	App	45h	Optional	Yes
Get User Name	22.29	App	46h	Optional	Yes
Set User Password	22.30	App	47h	Optional	Yes
Activate Payload	24.1	App	48h	-	Yes
Deactivate Payload	24.2	App	49h	-	Yes
Get Payload Activation Status	24.4	App	4Ah	-	No
Get Payload Instance Info	24.5	App	4Bh	-	No
Set User Payload Access	24.6	App	4Ch	-	Yes
Get User Payload Access	24.7	App	4Dh	-	Yes
Get Channel Payload Support	24.8	App	4Eh	-	No
Get Channel Payload Version	24.9	App	4Fh	-	No
Get Channel OEM Payload Info	24.10	App	50h	-	No
Master Write-Read	22.11	App	52h	Mandatory	Yes
Get Channel Cipher Suites	22.15	App	54h	-	Yes
Suspend/Resume Payload Encryption	24.3	App	55h	-	No
Set Channel Security Keys	22.25	App	56h	-	Yes
Get System Interface Capabilities	22.9	App	57h	-	No

F.1.4 Chassis Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Chassis Capabilities	28.1	Chassis	00h	Mandatory	Yes
Get Chassis Status	28.2	Chassis	01h	Optional/Mandatory	No
Chassis Control	28.3	Chassis	02h	Optional/Mandatory	Yes
Chassis Reset	28.4	Chassis	03h	Optional	Yes
Chassis Identify	28.5	Chassis	04h	Optional	No
Set Front Panel Button Enables	28.6	Chassis	0Ah	-	No
Set Chassis Capabilities	28.7	Chassis	05h	Optional	No
Set Power Restore Policy	28.8	Chassis	06h	Optional	Yes
Set Power Cycle Interval	28.9	Chassis	0Bh	-	No
Get System Restart Cause	28.11	Chassis	07h	Optional	No
Set System Boot Options	28.12	Chassis	08h	Optional	Yes
Get System Boot Options	28.13	Chassis	09h	Optional	Yes
Get POH Counter	28.14	Chassis	0Fh	Optional	No

F.1.5 Event Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Set Event Receiver	29.1	S/E	00h	Mandatory	Yes
Get Event Receiver	29.2	S/E	01h	Mandatory	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	02h	Mandatory	Yes

F.1.6 PEF and Alerting Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get PEF Capabilities	30.1	S/E	10h	Mandatory	No
Arm PEF Postpone Timer	30.2	S/E	11h	Mandatory	No
Set PEF Configuration Parameters	30.3	S/E	12h	Mandatory	No
Get PEF Configuration Parameters	30.4	S/E	13h	Mandatory	No
Set Last Processed Event ID	30.5	S/E	14h	Mandatory	No
Get Last Processed Event ID	30.6	S/E	15h	Mandatory	No
Alert Immediate	30.7	S/E	16h	Optional	No
PET Acknowledge	30.8	S/E	17h	Optional	No

F.1.7 Sensor Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Device SDR Info	35.2	S/E	20h	Optional	Yes
Get Device SDR	35.3	S/E	21h	Optional	Yes
Reserve Device SDR Repos-itory	35.4	S/E	22h	Optional	Yes
Get Sensor Reading Factors	35.5	S/E	23h	Optional	No
Set Sensor Hysteresis	35.6	S/E	24h	Optional	No
Get Sensor Hysteresis	35.7	S/E	25h	Optional	No
Set Sensor Threshold	35.8	S/E	26h	Optional	Yes
Get Sensor Threshold	35.9	S/E	27h	Optional	Yes
Set Sensor Event Enable	35.10	S/E	28h	Optional	Yes
Get Sensor Event Enable	35.11	S/E	29h	Optional	Yes
Re-arm Sensor Events	35.12	S/E	2Ah	Optional	Yes
Get Sensor Event Status	35.13	S/E	2Bh	Optional	Yes
Get Sensor Reading	35.14	S/E	2Dh	Mandatory	Yes
Set Sensor Type	35.15	S/E	2Eh	Optional	No
Get Sensor Type	35.16	S/E	2Fh	Optional	No

F.1.8 FRU Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get FRU Inventory Area Info	34.1	Storage	10h	Mandatory	Yes
Read FRU Data	34.2	Storage	11h	Mandatory	Yes
Write FRU Data	34.3	Storage	12h	Mandatory	Yes

F.1.9 SDR Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get SDR Repository Info	33.9	Storage	20h	Mandatory	Yes
Get SDR Repository Allocation Info	33.10	Storage	21h	Optional	No
Reserve SDR Repository	33.11	Storage	22h	Mandatory	Yes
Get SDR	33.12	Storage	23h	Mandatory	Yes
Add SDR	33.13	Storage	24h	Mandatory	No
Partial Add SDR	33.14	Storage	25h	Mandatory	No
Delete SDR	33.15	Storage	26h	Optional	No
Clear SDR Repository	33.16	Storage	27h	Mandatory	Yes
Get SDR Repository Time	33.17	Storage	28h	Optional/Mandatory	Yes
Set SDR Repository Time	33.18	Storage	29h	Optional/Mandatory	Yes
Enter SDR Repository Update Mode	33.19	Storage	2Ah	Optional	No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	Mandatory	No
Run Initialization Agent	33.21	Storage	2Ch	Optional	No

F.1.10 SEL Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get SEL Info	31.2	Storage	40h	Mandatory	Yes
Get SEL Allocation Info	31.3	Storage	41h	Optional	No
Reserve SEL	31.4	Storage	42h	Optional	Yes
Get SEL Entry	31.5	Storage	43h	Mandatory	Yes
Add SEL Entry	31.6	Storage	44h	Mandatory	Yes
Partial Add SEL Entry	31.7	Storage	45h	Mandatory	No
Delete SEL Entry	31.8	Storage	46h	Optional	No
Clear SEL	31.9	Storage	47h	Mandatory	Yes
Get SEL Time	31.10	Storage	48h	Mandatory	Yes
Set SEL Time	31.11	Storage	49h	Mandatory	Yes
Get Auxiliary Log Status	31.12	Storage	5Ah	Optional	No
Set Auxiliary Log Status	31.13	Storage	5Bh	Optional	No

F.1.11 LAN Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Set LAN Configuration Parameters	23.1	Transport	01h	Optional/Mandatory	Yes
Get LAN Configuration Parameters	23.2	Transport	02h	Optional/Mandatory	Yes
Suspend BMC ARPs	23.3	Transport	03h	Optional/Mandatory	No
Get IP/UDP/RMCP Statistics	23.4	Transport	04h	Optional	No

F.1.12 Serial/Modem Device Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Set Serial/Modem Configuration	25.1	Transport	10h	Optional/Mandatory	No
Get Serial/Modem Configuration	25.2	Transport	11h	Optional/Mandatory	No
Set Serial/Modem Mux	25.3	Transport	12h	Optional	No
Get TAP Response Codes	25.4	Transport	13h	Optional	No
Set PPP UDP Proxy Transmit Data	25.5	Transport	14h	Optional	No
Get PPP UDP Proxy Transmit Data	25.6	Transport	15h	Optional	No
Send PPP UDP Proxy Packet	25.7	Transport	16h	Optional	No
Get PPP UDP Proxy Receive Data	25.8	Transport	17h	Optional	No
Serial/Modem Connection Active	25.9	Transport	18h	Optional/Mandatory	No
Callback	25.10	Transport	19h	Optional	No
Set User Callback Options	25.11	Transport	1Ah	Optional	No
Get User Callback Options	25.12	Transport	1Bh	Optional	No
SOL Activating	26.1	Transport	20h	-	Yes
Set SOL Configuration Parameters	26.2	Transport	21h	-	Yes
Get SOL Configuration Parameters	26.3	Transport	22h	-	Yes

F.1.13 Bridge Management Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Bridge State	[ICMB]	Bridge	00h	Optional/Man-datory	No
Set Bridge State	[ICMB]	Bridge	01h	Optional/Man-datory	No
Get ICMB Address	[ICMB]	Bridge	02h	Optional/Man-datory	No
Set ICMB Address	[ICMB]	Bridge	03h	Optional/Man-datory	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	Optional/Man-datory	No
Get Bridge Statistics	[ICMB]	Bridge	05h	Optional/Man-datory	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	Optional/Man-datory	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	Optional/Man-datory	No
Get Bridge Proxy Address	[ICMB]	Bridge	09h	Optional/Man-datory	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	Optional/Man-datory	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	Optional/Man-datory	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	Optional/Man-datory	No

F.1.14 Discovery Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Prepare For Discovery	[ICMB]	Bridge	10h	Optional/Man-datory	No
Get Addresses	[ICMB]	Bridge	11h	Optional/Man-datory	No
Set Discovered	[ICMB]	Bridge	12h	Optional/Man-datory	No
Get Chassis Device ID	[ICMB]	Bridge	13h	Optional/Man-datory	No
Set Chassis Device ID	[ICMB]	Bridge	14h	Optional/Man-datory	No

F.1.15 Bridging Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Bridge Request	[ICMB]	Bridge	20h	Optional/Man-datory	No
Bridge Message	[ICMB]	Bridge	21h	Optional/Man-datory	No

F.1.16 Event Commands (ICMB)

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get Event Count	[ICMB]	Bridge	30h	Optional/Man-datory	No
Set Event Destination	[ICMB]	Bridge	31h	Optional/Man-datory	No
Set Event Reception State	[ICMB]	Bridge	32h	Optional/Man-datory	No
Send ICMB Event Message	[ICMB]	Bridge	33h	Optional/Man-datory	No
Get Event Destination	[ICMB]	Bridge	34h	Optional/Man-datory	No
Get Event Reception State	[ICMB]	Bridge	35h	Optional/Man-datory	No

F.1.17 OEM Commands for Bridge NetFn

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
OEM Commands	[ICMB]	Bridge	C0h-FEh	Optional/Man-datory	No

F.1.18 Other Bridge Commands

Command	IPMI v2.0 Ref.	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Error Report	[ICMB]	Bridge	FFh	Optional/Man-datory	No

F.2 PICMG IPMI Commands

F.2.1 AdvancedTCA (PICMG 3.0 R3.0 AdvancedTCA Base Specification)

Command	PICMG 3.0 Table	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get PICMG Properties	3-11	PICMG	00h	-	Yes
Get Address Info	3-10	PICMG	01h	-	No
Get Shelf Address Info	3-16	PICMG	02h	-	No
Set Shelf Address Info	3-17	PICMG	03h	-	No
FRU Control	3-27	PICMG	04h	-	Yes
Get FRU LED Properties	3-29	PICMG	05h	-	Yes
Get LED Color Capabilities	3-30	PICMG	06h	-	Yes
Set FRU LED State	3-31	PICMG	07h	-	Yes
Get FRU LED State	3-32	PICMG	08h	-	Yes
Set IPMB State	3-70	PICMG	09h	-	No
Set FRU Activation Policy	3-20	PICMG	0Ah	-	No
Get FRU Activation Policy	3-21	PICMG	0Bh	-	No
Set FRU Activation	3-19	PICMG	0Ch	-	No
Get Device Locator Record ID	3-39	PICMG	0Dh	-	Yes
Set Port State	3-59	PICMG	0Eh	-	No
Get Port State	3-60	PICMG	0Fh	-	No
Compute Power Properties	3-82	PICMG	10h	-	No
Set Power Level	3-84	PICMG	11h	-	No
Get Power Level	3-83	PICMG	12h	-	No
Renegotiate Power	3-91	PICMG	13h	-	No
Get Fan Speed Properties	3-86	PICMG	14h	-	No
Set Fan Level	3-88	PICMG	15h	-	No
Get Fan Level	3-87	PICMG	16h	-	No
Bused Resource	3-62	PICMG	17h	-	No
Get IPMB Link Info	3-68	PICMG	18h	-	No
Get Shelf Manager IPMB Address	3-38	PICMG	1Bh	-	No
Set Fan Policy	3-89	PICMG	1Ch	-	No
Get Fan Policy	3-90	PICMG	1Dh	-	No
FRU Control Capabilities	3-26	PICMG	1Eh	-	Yes
FRU Inventory Device Lock Control	3-42	PICMG	1Fh	-	No
FRU Inventory Device Write	3-43	PICMG	20h	-	No
Get Shelf Manager IP-Addresses	3-36	PICMG	21h	-	No
Get Shelf Power Allocation	3-85	PICMG	22h	-	No
Get Telco Alarm Capability	3-93	PICMG	29h	-	No
Set Telco Alarm State	3-94	PICMG	2Ah	-	No
Get Telco Alarm State	3-95	PICMG	2Bh	-	No
Get Telco Alarm Location	3-96	PICMG	39h	-	No
Set FRU Extracted	3-25	PICMG	3Ah	-	No

F.2.2 HPM.1 (R1.0)

Command	HPM.1 Table	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Get target upgrade capabilities	3-3	PICMG	2Eh	-	Yes
Get component properties	3-5	PICMG	2Fh	-	Yes
Abort Firmware Upgrade	3-15	PICMG	30h	-	Yes
Initiate upgrade action	3-8	PICMG	31h	-	Yes
Upload firmware block	3-9	PICMG	32h	-	Yes
Finish firmware upload	3-10	PICMG	33h	-	Yes
Get upgrade status	3-2	PICMG	34h	-	Yes
Activate firmware	3-11	PICMG	35h	-	Yes
Query Self-test Results	3-12	PICMG	36h	-	Yes
Query Rollback status	3-13	PICMG	37h	-	Yes
Initiate Manual Rollback	3-14	PICMG	38h	-	Yes

F.3 OEM/Group IPMI Commands

F.3.1 Advantech OEM Commands

Command	NetFn	CMD	IPMI BMC Req.	Advantech BMC support
Store Configuration Settings	OEM/Group	40h	-	Yes
Read Configuration Settings	OEM/Group	41h	-	Yes
Read Port 80	OEM/Group	80h	-	Yes
Clear NVRAM Data	OEM/Group	81h	-	Yes
Read MAC Address	OEM/Group	E2h	-	Yes
Load Default Configuration	OEM/Group	F2h	-	Yes

Appendix G

Driver & Tools

G.1 OpenIPMI

The OpenIPMI project provides an IPMI Kernel driver which is available in most of the Linux distributions.

The Open IPMI Linux device driver is designed as a full-function IPMI device driver with the following features:

- Allows multiple users.
- Allows multiple interfaces.
- Allows both kernel and userland things to use the interface.
- Fully supports the watchdog timer.
- It works like IPMI drivers are supposed to. It tracks outgoing messages and matches up their responses automatically. It automatically fetches events, received messages, etc.
- It supports interrupts (I have tested them now).
- It has backwards-compatibility modules for supporting the Radisys IPMI driver and the Intel IMB driver.
- It's modular. You don't have to have the standard userland interface. You don't have to have the watchdog. Etc.
- It supports generating an event on a panic.

Source: OpenIPMI Page (http://openipmi.sourceforge.net/)

More information regarding the IPMI driver can be found on the OpenIPMI Project page, http://openipmi.sourceforge.net/

The KCS register interfaces are at 0xCA2 /0xCA3 and used by the OpenIPMI driver as default.

G.2 IPMITool

The IPMITool provides an easy-to-use set of functions and commands, to access the BMC via the KCS interface within the Operating System of the MIC-6330 or via Ethernet through NC-SI from external. The IPMI Tool also supports bridged IPMI commands to access the BMC, if the carrier manager provides an IPMI-over-LAN interface. See Chapter 3 & 4 for a more detailed description of different access methods and IPMITool calls.

The IPMITool source code can be downloaded from the official project page, http://ipmitool.sourceforge.net.

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